

High Performance Low Density Parity Check (LDPC) Decoder for Chinese Digital TV Standard

Vijay Kumar t. Korishetti, Nitin b.Sambre

Abstract:- This paper proposes an LDPC decoder of forward error correction (FEC), for the Chinese digital terrestrial television multimedia broadcasting (CDTMB) standard, based on Log domain Sum product algorithm (SPA) decoder. The LDPC FEC encoding for CDTMB includes three kinds of code rates with a code word block size of 7493. The simulated LDPC decoder consumes less power as the hardware complexity is reduced. The results obtained also indicate better Bit Error Rate (BER) for low Signal to Noise ratio (SNR).

Keywords: LDPC codes, DTV, Log SPA, FEC, LLR.

I. INTRODUCTION

LDPC codes were discovered by Robert Gallager [1] in the 1960's. They were forgotten for almost 30 years before being rediscovered again in the mid-1990. LDPC codes were resurrected with the contribution of Mackay and Neal. The remarkable error correction performance and low implementation complexity of LDPC codes led to their recent inclusion in broadcasting systems, such as next generation digital video broadcasting via satellite (DVB-T2) [2], and have been optional FEC techniques in networks, such as Wireless-LAN (802.11n) [10] and Wireless-MAN (IEEE 802.16e) [10], etc. The most important advantage, of LDPC codes is they allow data transmission rates close to the Shannon limit that is the theoretical rate. LDPC are linear block codes defined by a sparse parity check matrix. The total number of ones in each row and column is smaller in comparison with the total elements of all rows and columns. The parity check matrix can be viewed as a bipartite graph with two kinds of nodes: check nodes corresponding to the rows and variable-nodes corresponding to the columns of the parity check matrix [4], as shown in Fig 1-

$$H = \begin{bmatrix} 1 & 1 & 1 & 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 & 1 & 1 & 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 1 & 0 & 0 & 1 & 1 & 0 \\ 0 & 0 & 1 & 0 & 0 & 1 & 0 & 1 & 0 & 1 \\ 0 & 0 & 0 & 1 & 0 & 0 & 1 & 0 & 1 & 1 \end{bmatrix}$$

In this paper, we present a CDTMB compliant LDPC decoder architecture based on Log-SPA that gives better error correcting capability with high performance. The rest of the paper is organized as follows. Section 2 presents FEC encoding details for Chinese Digital TV standard. Section 3 briefs the Log domain SPA algorithm. Section 4 describes the simulation and implementation results. Finally section 5 concludes the paper.

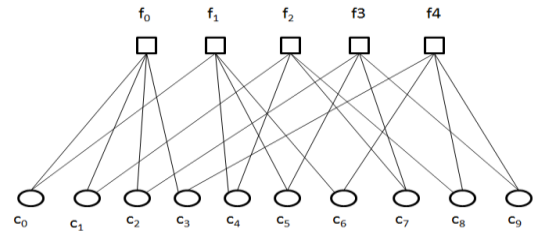


Fig. 1. Bipartite Graph for Above Example

II. FEC ENCODING SCHEME FOR CDTMB

In CDTMB Standard [3] three code rates of LDPC decoder are used namely-0.4, 0.6, and 0.8. The codeword length for all the code rates remain constant as 7493. The parity matrix details for these code rates is defined as follows-

$$H = \begin{bmatrix} B_{0,0} & B_{0,1} & \cdots & B_{0,c-1} \\ B_{1,0} & B_{1,1} & \cdots & B_{1,c-1} \\ \vdots & \vdots & \vdots & \vdots \\ B_{r-1,0} & B_{r-1,1} & \cdots & B_{r-1,c-1} \end{bmatrix}$$

Here $B_{i,j}$ is a base matrix of size 127x127. If $B_{i,j} = n$, it means n^{th} column of the first row contains 1 and other elements of base matrix are 0. Including the second row, remaining 126 row are right cyclic shift of the previous row. The value of n is previously defined [3]. Table I gives the details of Parity check matrix parameters for Chinese standard for the three code rates.

Table 1. Coding Parameters of Parity Check Matrix

Code rate	Codeword length	Information bits	Parity bits
0.4	7493	3048	4445
0.6	7493	4572	2921
0.8	7493	6096	1397

With these details the parity matrix construction and the encoding of data shall be achieved as per guidelines in CDTMB reference manual [3].

III. DECODING USING SPA DECODER

SPA decoder is derived from probability domain decoder [4], to reduce the number of multiplications involved in decoding process as products are costly to implement on hardware and also repeated products of probabilities make the decoder unstable. The calculation complexities are

reduced using $\phi(x) = -\log[\tanh(x/2)]$ property of SPA method [4]. The summary of equations for Log SPA is as follows-

Step 1 Initialization:

The LLR value of the received symbol Y_i is initialized to the corresponding variable nodes $L(c_i)$ using Equation 1 and associate these $L(c_i)$ values with nonzero elements of parity check matrix H using Equation 2.

$$L(c_i) = \text{LLR}(Y_i) \tag{1}$$

$$L(q_{ij}) = H \cdot L(c_i) \tag{2}$$

$$L(r_{ji}) = 0 \tag{3}$$

Where,

$$L(c_i) = \text{LLR value of input bit } Y_i = \text{Log} \left[\frac{\Pr(c_i = 0 | Y)}{\Pr(c_i = 1 | Y)} \right]$$

$$L(q_{ij}) = \text{Log} \left[\frac{q_{ij}(0)}{q_{ij}(1)} \right]$$

$$L(r_{ji}) = \text{Log} \left[\frac{r_{ji}(0)}{r_{ji}(1)} \right]$$

Step 2 Horizontal scan (Check node update)

$$L(r_{ji}) = \prod_{i' \in V_j \setminus i} \alpha_{i'j} \cdot \phi \left(\sum_{i' \in V_j \setminus i} \phi(\beta_{i'j}) \right) \tag{4}$$

Where,

$$\phi(x) = -\log[\tanh(x/2)]$$

$$\alpha_{ij} = \text{Sign}[L(q_{ij})]$$

$$\beta_{ij} = |L(q_{ij})|$$

Step 3 Vertical Scan (Variable node update)

$$L(q_{ij}) = L(c_i) + \sum_{j' \in c_i \setminus j} L(r_{ji'}) \tag{5}$$

Step 4 Decision Loop

$$L(Q_i) = L(c_i) + \sum_{j \in c_i} L(r_{ji}) \tag{6}$$

$$c_i = 1 \text{ if } L(Q_i) > 0, 0 \text{ elsewhere}$$

Decoding process stops one the parity check $H \cdot C^T = 0$ is met otherwise go to step 2.

IV. SIMULATION RESULTS

Fig 2, Fig 3, Fig 4 shows the bit error rates (BER) performance versus signal-to-noise ratio E_b/N_0 , over an AWGN channel for proposed CDTMB standard Log SPA LDPC decoder. This simulation are for the block size of 7493 and is run for the code rates 0.4, 0.6 and 0.8 with QAM 4 modulation scheme, for 20 iterations. The results plotted meet the CDTMB requirement and proves the high error correcting capability of SPA codes in comparison with Single scan Min sum algorithm.

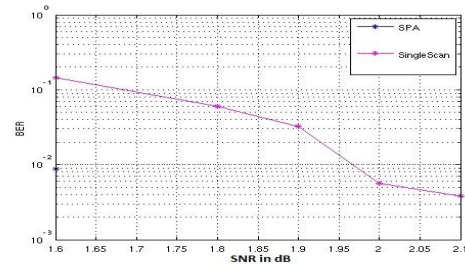


Fig 2. BER Performance Curve for 0.4 Code Rate with QAM-4

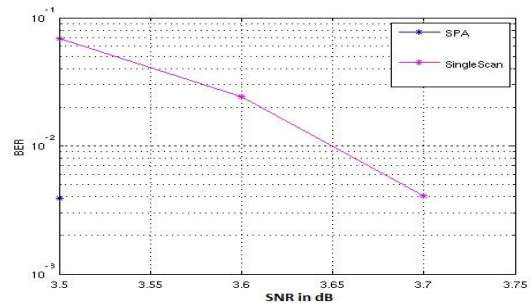


Fig 3. BER Performance Curve for 0.6 Code Rate with QAM-4

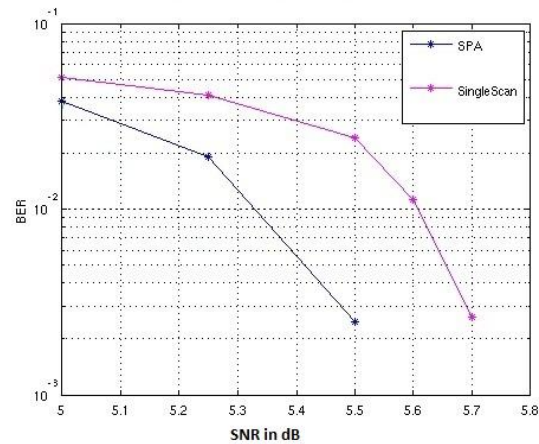


Fig 4. BER Performance Curve for 0.8 Code Rate with QAM-4

V. CONCLUSION

In this paper we present the implementation and evaluation of LDPC decoder for the CDTMB standard using Log-Domain SPA. It is seen by the simulation that this

algorithm has better error correcting capabilities. The results also show that the BER performance of LDPC decoder is close to Shannon limit.

VI. ACKNOWLEDGEMENT

We would like to thank Mr. Abhijeet Magdum from Saankhya Labs Pvt. Ltd, Bangalore for his continuous support and guidance throughout the experimental process regarding this research work and reviewing this research paper. He is having a total industrial experience of 5 years in Communications domain.

REFERENCES

- [1] R. G. Gallager, Low-Density Parity-Check Codes. Cambridge, MA: MIT Press, 1963.
- [2] ETSI, "Digital Video Broadcasting (DVB)", ETSI EN 302 755 V1.1.1 (2009-09).
- [3] GB 20600-2006 - Framing structure, channel coding and modulation for Digital Terrestrial Television Broadcasting.
- [4] William E. Ryan, "An Introduction to LDPC Codes", August 19, 2003.
- [5] Xiaofei Huang, "Single-Scan Min-Sum Algorithms for fast decoding of LDPC Codes ", IEEE Information Theory Workshop, Chengdu, China, 2006.
- [6] Mohammad M. Mansour, " High-Throughput LDPC Decoders", IEEE transactions on very large scale integration systems, vol. 11, no. 6, December 2003.
- [7] Van Ying, Dan Bo, Shuangqu Huang, Bo Xiang, Yun Chen *, Xiao yang Zeng *, " A Cost efficient LDPC decoder for DVB-S2.
- [8] Zhiqiang Cui, Zhongfeng Wang, and Youjian (Eugene) Liu, " High-Throughput Layered LDPC Decoding Architecture", IEEE transactions on very large scale integration (VLSI) systems, vol. 17, no. 4, April 2009.
- [9] Haeseong Jeong, Jong Tae Kim, " Implementation of LDPC Decoder in DVB-S2 Using Min-Sum Algorithm", International Conference on Convergence and Hybrid Information Technology 2008.
- [10] Z. Cai, J. Hao, P.H. Tan, S. Sun and P.S. Chin, " Efficient encoding of IEEE 802.11n LDPC.