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DCT Based Improved OFDM Communication

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Abstract*— to improve the performance of a system is the best criteria for developing any communication system. The work presented here targets increasing the speed & performance of the OFDMA (Orthogonal Frequency-Division Multiple Access) modulator and demodulator. This paper presents a high level implementation of a high performance DCT for OFDM Modulator and Demodulator, with fewer computational steps than some other transforms. The design has been coded in VHDL and put into Xilinx Spartan3 FPGAs. The developed OFDMA communication structure can then be targeted to the OFDMA based WiMAX and other wireless communication systems, for increasing their efficiency by utilizing FPGA based DCT algorithm.

Keywords: **DCT, FPGA, OFDMA, QAM, VHDL.**

I. INTRODUCTION TO OFDM

OFDM (Orthogonal Frequency-Division Multiplexing) is a modulation technique which makes good use of available bandwidth by allocating orthogonal sub carriers. OFDM is a parallel data-transmission scheme, which reduces the influence of multipath fading and supports high rates without the need of conventional equalization techniques. OFDM is a special case of multicarrier transmission, where a single data stream is transmitted over a number of lower-rate subcarriers. The implementation complexity is significantly lower than that of a single-carrier system with an equalizer. OFDM is robust against narrowband interference because such interference affects only a small percentage of the subcarriers; it also increases robustness against frequency-selective fading. OFDM is used in physical layer of various wireless standards such as IEEE 802.11a, IEEE 802.16a, and HIPERLAN/2, DAB, DVB. All these commercially used schemes use discrete transforms to generate orthogonal subcarriers [1]. OFDM exploits the frequency diversity of the multipath mobile broadband channel by coding and interleaving the information across the subcarriers prior to transmission. After organizing the time and frequency resources in an OFDMA system into resource blocks for allocation to the individual mobile stations, the coded and interleaved information bits of a specific mobile station are modulated onto the subcarriers of its resource blocks.

II. DISCRETE COSINE TRANSFORM

The sequences normally used in any sort of transform from one domain to the other are referred to as the basis sequences, and these are complex periodic sequences in case of Discrete Fourier Transform. Thus, it is important to find out if there exists some real valued basis sequences that would result in a real valued transform sequence. This is ended up in finding up of a lot of other transforms, which are all orthogonal transforms, such as Hadamard Transform, Haar Transform, Hartley Transform etc. But there is another transform which is quite closely related to the DFT, which is called the Discrete Cosine Transform or DCT. A Discrete Cosine Transform (DCT) expresses a sequence of finitely many data points in terms of a sum of cosine functions oscillating at different frequencies. DCTs are important to numerous applications in science and engineering, from lossy compression of audio (e.g. MP3) and images (e.g. JPEG) where small high-frequency components can be discarded. The most common variant of discrete cosine transform is the type-II DCT, which is often called simply "the DCT" and its inverse, the type-III DCT, is correspondingly often called simply "The inverse DCT" or "the IDCT". The use of cosine rather than sine functions is critical in these applications: for compression, it turns out that cosine functions are much more efficient as fewer functions are needed to approximate a typical signal. In particular, a DCT is a Fourier-related transform similar to the discrete Fourier transform (DFT), but using only real numbers.

III. FAST FOURIER TRANSFORM

A Fast Fourier transform (FFT) is an algorithm to compute the discrete Fourier transform (DFT) and it's inverse. The DFT is obtained by decomposing a sequence of values into components of different frequencies. OFDM can be easily and quite effectively implemented using FFT as well. The FFT algorithm eliminates the redundant calculation which is needed in computing Discrete Fourier Transform (DFT) and is thus very suitable for efficient hardware implementation [2].

IV. OFDM SYSTEM: FFT BASED

To generate OFDM successfully the relationship between all the carriers must be carefully controlled to maintain the orthogonality of the carriers. For this reason, OFDM is generated by firstly choosing the spectrum required, based on the input data, and modulation scheme used. Each carrier to be produced is assigned some data to transmit. The required amplitude and phase of the carrier is then calculated based on the modulation scheme (typically differential BPSK, QPSK, or QAM). The multiple orthogonal subcarrier signals, which are overlapped in spectrum, need to be produced at the transmitter side. In practice, Discrete Fourier Transform (DFT) and Inverse DFT (IDFT) processes are useful for implementing these orthogonal signals. DFT and IDFT can be implemented efficiently by using fast Fourier transform (FFT) and inverse fast Fourier transform (IFFT), respectively. In the OFDM transmission system,

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N point IFFT is taken for the transmitted symbols so as to generate, the samples for the sum of N orthogonal subcarrier signals. The receiver will receive a sample corrupted by additive noise. Taking the N-point FFT of the received samples the noisy version of transmitted symbols can be obtained in the receiver. The spectrum of the OFDM signal can be considered as the sum of the frequency shifted sinc functions in the frequency domain because all subcarriers are of the finite duration. The OFDM scheme also inserts a guard interval in the time domain, called cyclic prefix (CP), which mitigates the inter-symbol interference (ISI) between OFDM symbols.

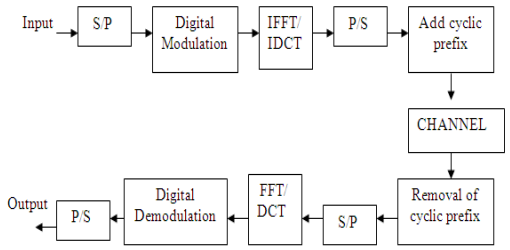

Fig 1 [8]: OFDM System Transmitter and Receiver [FFT/DCT]

Fig. 1 shows the configuration for a basic OFDM transmitter and receiver. The signal generated is at baseband and so to generate an RF signal the signal must be filtered and mixed to the desired transmission frequency [3]. The sequence of N complex numbers x_0... x_{N-1} is transformed into the sequence of N complex numbers X_0... X_{N-1} by the DFT according to the Eq. (1) below.

$$X_K = \sum_{n=0}^{N-1} x_n e^{\frac{-2\pi i}{N} kn} \quad (1)$$

Where i is the imaginary unit and is a primitive Nth root of unity and k = 0... N-1. The Inverse Discrete Fourier Transform (IDFT) is given by Eq. (2)

$$x_n = \frac{1}{N} \sum_{k=0}^{N-1} X_k e^{\frac{-2\pi i}{N} kn} \quad (2)$$

Where n = 0... N-1

A simple description of these equations is that the complex numbers Xk represent the amplitude and phase of the different sinusoidal components of the input signal xn. The DFT computes the Xk from the xn, while the IDFT shows how to compute the xn as a sum of sinusoidal components found with frequency k/N cycles per sample.

A key enabling factor for these applications is the fact that the DFT can be computed efficiently in practice using a Fast Fourier Transform (FFT) algorithm. "DFT" refers to a mathematical transformation or function, regardless of how it is computed, whereas "FFT" refers to a specific family of algorithms for computing DFTs.

V. OFDM SYSTEM: DCT BASED.

Instead of using complex exponential functions, cosinusoidal functions can be used as orthogonal basis to implement multi-carrier scheme [6]. This can be synthesized using discrete cosine transform (DCT). For fast implementation algorithms DCT can provide fewer computational steps than FFT based OFDM. The effect of carrier frequency offset (CFO) will introduce inter-carrier interference (ICI) in both the DFT-OFDM and DCT-OFDM. A single co sinusoidal functions set $\cos 2\pi NrF\Delta t$ will be used as the orthogonal basis to implement MCM in DCT-OFDM. The minimum $F\Delta$ required to satisfy Eq. (3) is 1/2T Hz.

$$\int_0^T \sqrt{\frac{2}{T}} \cos(2\pi F_\Delta t) \sqrt{\frac{2}{T}} \cos(2\pi m F_\Delta t)\, dt = \begin{cases} 1, k = m \\ 0, k \neq m \end{cases} \quad (3)$$

A zero-padding guard-interval scheme should be used in a DCT-OFDM system. The zero-padding scheme will eliminate ISI, and also improve transmission efficiency. DFT-OFDM shows that the zero-padded (ZP) DFT-OFDM can achieve a better BER performance than cyclic prefix (CP) DFT-OFDM. Same is the case with respect to the DCT-OFDM.

A. The Block Diagram

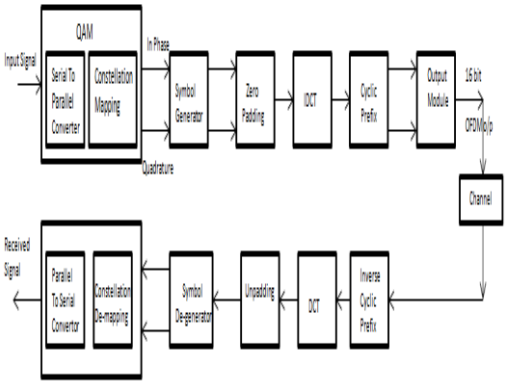

Fig 2: Block Diagram for Improved DCT Based OFDM System

The above block diagram based implementation involves separate sets of blocks which are:

- QAM - Serial to parallel converter.
- Constellation Mapping.
- Symbol Generator.
- Inverse Discrete Cosine Transform.
- Cyclic Prefix.
- Output Module for OFDM output.
- The Channel
- Inverse Cyclic Prefix
- Discrete Cosine Transform
- Symbol De-generator
- QAM – Parallel to Serial Converter
- Constellation De-mapping

The implementation of DCT based OFDM on FPGA is being done on Spartan 3 XC3S400PQ208.

B. Implementation Details

- QAM (Quadrature Amplitude Modulation)

Quadrature amplitude modulation (QAM) is both an analog and a digital modulation scheme. It conveys two analog message signals, or two digital bit streams, by changing (modulating) the amplitudes of two carrier waves, using the amplitude-shift keying (ASK) digital

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modulation scheme or amplitude modulation (AM) analog modulation scheme. The two carrier waves, usually sinusoids, are out of phase with each other by 90° and are thus called quadrature carriers or quadrature components — hence the name of the scheme. The modulated waves are summed, and the resulting waveform is a combination of both phase-shift keying (PSK) and amplitude-shift keying (ASK), or (in the analog case) of phase modulation (PM) and amplitude modulation. In the digital QAM case, a finite number of at least two phases and at least two amplitudes are used. PSK modulators are often designed using the QAM principle, but are not considered as QAM since the amplitude of the modulated carrier signal is constant. QAM is used extensively as a modulation scheme for digital telecommunication systems. QAM divides a signal into two parts, which are the In-phase and the Quadrature components. The In-phase and Quadrature component separates the incoming signal to real and imaginary parts, and are 90 degrees out of phase.

Serial to Parallel Converter – The Serial to Parallel Converter converts the incoming serial data into parallel In-phase and Quadrature components which are 90 degrees out of phase so that real part can be separated from the imaginary part and a faster transmission can be achieved.

Constellation Mapping and De-mapping – The QAM technique involves constellation mapping of signal components using constellation diagram. A constellation diagram is a representation of a signal modulated by a digital modulation scheme such as quadrature amplitude modulation or phase-shift keying. By representing a transmitted symbol as a complex number and modulating a cosine and sine carrier signal with the real and imaginary parts (respectively), the symbol can be sent with two carriers on the same frequency. On the contrary, De-mapping just de-maps the constellation binary symbol components back to their original binary form.

The constellation diagram for 16 bit QAM can be shown as below.

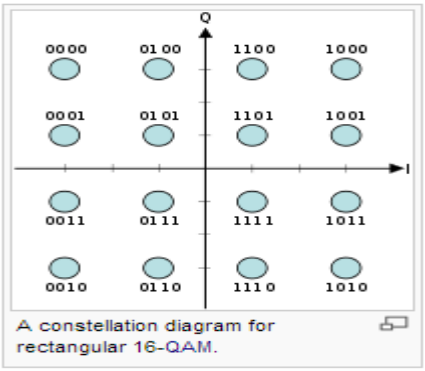

Fig 3 [9]: Constellation diagram for 16 bit QAM

- Symbol Generator and De-Generator.

The symbol generator validates the input given to it and generates valid symbols only to be passed on the DCT block. These symbols are binary symbols of course. The de-generator just converts the received noisy signal in the form required to be an input for the QAM block.

- Zero Padding and Un-padding.

Zero Padding is a technique involved to separate streams of data. The stream of data is padded with zeros both before and after the data, so that every two streams of data is separated and a proper transform can be performed. In this implementation, zero padding is 32 bits wide. So, every data stream, which is 64 bits, has 32 plus 32 zero padded bits ahead of and after it respectively.

- DCT and Inverse Discrete Cosine Transform (IDCT).

The multiple orthogonal subcarrier signals, which are overlapped in spectrum, need to be produced at the transmitter side. In practice, Discrete Cosine Transform (DCT) and Inverse DCT (IDCT) processes are useful for implementing these orthogonal signals. In the OFDM transmission system, N point IDCT is taken for the transmitted symbols so as to generate the samples for the sum of N orthogonal subcarrier signals. The receiver will receive a sample corrupted by additive noise. Taking the N-point DCT of the received samples the noisy version of transmitted symbols can be obtained in the receiver. The spectrum of the OFDM signal can be considered as the sum of the frequency shifted cosine functions in the frequency domain because all subcarriers are of the finite duration.

- Cyclic Prefix and Inverse Cyclic Prefix.

The OFDM scheme also inserts a guard interval in the time domain, called cyclic prefix (CP), which mitigates the inter-symbol interference (ISI) between OFDM symbols. Once the signal is received by the receiver, the effect of ISI is over and thus the cyclic prefix is removed by using Inverse Cyclic Prefix [5].

- Output Module for OFDM output.

The Output Module acts as an OFDM signal generating module, which apart from generating the OFDM output, filters the unwanted cosine terms from the Cyclic prefixed data. This OFDM output is passed on to the receiver through the channel.

- The Channel.

The channel is just a transmission medium between the transmitter and the receiver in which the data flows. The OFDM output generated is passed on to
the receiver through the channel.

- Parallel to Serial Converter.

The Parallel to Serial Converter converts the incoming parallel data components which are 90 degrees out of phase into serial output data so that it matches the input data destined for the receiver, along with noise signals.

C. HARDWARE AND SOFTWARE REQUIREMENTS:

HARDWARE:

- FPGA

A field-programmable gate array (FPGA) is an integrated circuit designed to be configured by a customer or a designer after manufacturing—hence "field-

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programmable". The FPGA configuration is generally specified using a hardware description language (HDL), similar to that used for an application-specific integrated circuit (ASIC) (circuit diagrams were previously used to specify the configuration, as they were for ASICs, but this is increasingly rare). FPGAs can be used to implement any logical function that an ASIC could perform. The ability to update the functionality after shipping, partial re-configuration of a portion of the design and the low non-recurring engineering costs relative to an ASIC design (notwithstanding the generally higher unit cost), offer advantages for many applications. FPGAs contain programmable logic components called "logic blocks", and a hierarchy of reconfigurable interconnects that allow the blocks to be "wired together"—somewhat like many (changeable) logic gates that can be inter-wired in (many) different configurations. Logic blocks can be configured to perform complex combinational functions, or merely simple logic gates like AND and XOR. In most FPGAs, the logic blocks also include memory elements, which may be simple flip-flops or more complete blocks of memory. Details and configuration of Spartan 3 has been explained in section below for Spartan 3. The architecture of Spartan 3 FPGA can be shown as below.

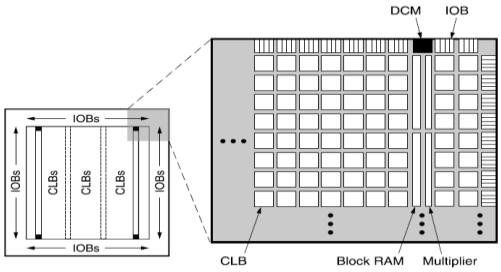

Fig 4: FPGA Architecture

Some FPGAs have analog features in addition to digital functions. The most common analog feature is programmable slew rate and drive strength on each output pin, allowing the engineer to set slow rates on lightly loaded pins that would otherwise ring unacceptably, and to set stronger, faster rates on heavily loaded pins on high-speed channels that would otherwise run too slow. Another relatively common analog feature is differential comparators on input pins designed to be connected to differential signalling channels. A few "mixed signal FPGAs" have integrated peripheral analog-to-digital converters (ADCs) and digital-to-analog converters (DACs) with analog signal conditioning blocks allowing them to operate as a system-on-a-chip. Such devices blur the line between an FPGA, which carries digital ones and zeros on its internal programmable interconnect fabric, and field-programmable analog array (FPAA), which carries analog values on its internal programmable interconnect fabric.

- FPGA Spartan 3

Configuration: Spartan-3 FPGAs are programmed by loading configuration data into robust, reprogrammable, static CMOS configuration latches (CCLs) that collectively control all functional elements and routing resources. Before powering on the FPGA, configuration data is stored externally in a PROM or some other non volatile medium either on or off the board. After applying power, the configuration data is written to the FPGA using any of five different modes: Master Parallel, Slave Parallel, Master Serial, Slave Serial, and Boundary Scan (JTAG). The Master and Slave Parallel modes use an 8-bit-wide Select MAP port. The recommended memory for storing the configuration data is the low-cost Xilinx Platform Flash PROM family, which includes the XCF00S PROMs for serial configuration and the higher density XCF00P PROMs for parallel or serial configuration.

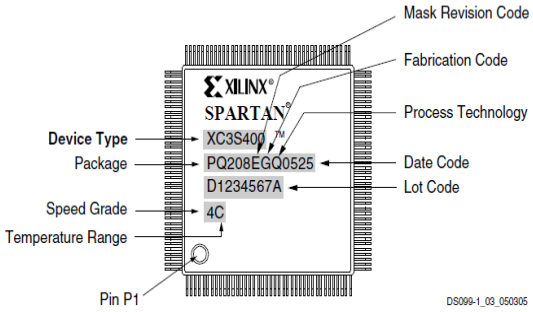

Fig 5: Spartan-3 Configuration

Features:

- Low-cost, high-performance logic solution for high-volume, consumer-oriented applications
- Densities up to 74,880 logic cells
- Select IO™ interface signalling
- Up to 633 I/O pins
- Logic resources
- Abundant logic cells with shift register capability
- Wide, fast multiplexers
- Fast look-ahead carry logic
- Dedicated 18 x 18 multipliers
- JTAG logic compatible with IEEE 1149.1/1532
- Automotive Spartan-3 XA Family variant.

SOFTWARE

- VHDL

The design has been coded in Very High Integrated Circuits Hardware Descriptive Language (VHDL) and targeted into Xilinx Spartan3 FPGAs. VHDL is very useful for quickly evaluating new algorithms in FPGA hardware [6]. VHDL is the VHSIC Hardware Description Language. VHSIC is an abbreviation for Very High Speed Integrated Circuit. It can describe the behaviour and structure of electronic systems, but is particularly suited as a language to describe the structure and behaviour of digital electronic hardware designs, such as ASICs and FPGAs as well as conventional digital circuits.

Technology

VHDL permits technology independent design through support for top down design and logic synthesis. To move a design to a new technology you need not start from

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scratch or reverse-engineer a specification - instead you go back up the design tree to a behavioural VHDL description, then implement that in the new technology knowing that the correct functionality will be preserved.

Benefits

- Executable specification
- Validate spec in system context (Subcontract)
- Functionality separated from implementation
- Simulate early and fast (Manage complexity)
- Explore design alternatives
- Get feedback (Produce better designs)
- Automatic synthesis and test generation (ATPG for ASICs)
- Increase productivity (Shorten time-to-market)
- Technology and tool independence (though FPGA features may be unexploited)
- Portable design data (Protect investment)

The simulation can be demonstrated in VHDL software ModelSim.

- ModelSim

ModelSim is a "High Performance and Capacity Mixed HDL Simulation Tool". Mentor Graphics was the first to combine single kernel simulator (SKS) technology with a unified debug environment for Verilog, VHDL, and System C. The combination of industry-leading, native SKS performance with the best integrated debug and analysis environment make ModelSim the simulator of choice for both ASIC and FPGA design. The best standards and platform support in the industry make it easy to adopt in the majority of process and tool flows.

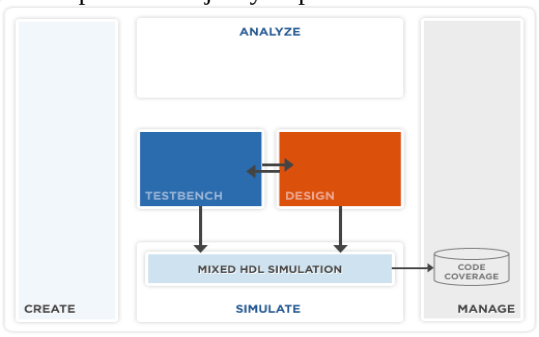

Fig 6: ModelSim tool flow

Overview

- Unified mixed language simulation engine for the fastest regression suite throughput
- Native support of Verilog, SystemVerilog for design, VHDL, and SystemC for effective verification of the most sophisticated design environments
- Fast time-to-debug causality tracing and multi-language debug environment
- Advanced code coverage and analysis tools for fast time to coverage closure.

Features

- Advanced Code Coverage:

ModelSim's advanced code coverage capabilities and ease of use lower the barriers for leveraging this valuable verification resource. The ModelSim advanced code coverage capabilities provide valuable metrics for systematic verification. All coverage information is stored in the Unified Coverage Data Base (UCDB), which is used to collect and manage all coverage information in a highly efficient database. Coverage utilities that analyze code coverage data, such as merging and test ranking, are available. Coverage results can be viewed interactively, post-simulation, or after a merge of multiple simulation runs. Code coverage metrics can be reported by instance or by design unit, providing flexibility in managing coverage data.

D. Comparison of DCT with FFT and DCT's advantages.

It has been found in previous researches that DCT is an efficient transform compared to FFT, since fewer steps are needed for its implementation. Moreover, DCT avoids complex exponential functions and uses only real values, unlike FFT which uses complex numbers. BER Comparison of both previously observed can be shown as in Fig. 6

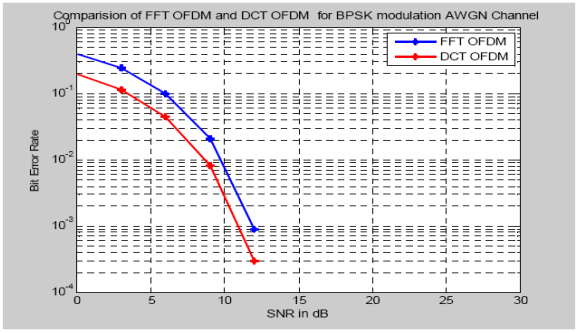

Fig. 7: BER performance of FFT Based OFDM and DCT Based OFDM for BPSK modulation and AWGN Channel.

From Fig. 6, it has been observed that BER performance of FFT –based OFDM in an AWGN environment outperform FFT -based OFDM.

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Her current research interests include Image Processing and Antenna Array Design. She is currently working as Assistant Professor at MVJ College