ISSN: 2277-3754
ISO 9001:2008 Certified
International Journal of Engineering and Innovative Technology (IJEIT)
Volume 2, Issue 12, June 2013

Process Aware Circuit Design Using Adaptive Body Biasing

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Abstract*—The process variation has become inevitable in the present VLSI technology. The IC designed without consideration of process variation fails to do operation correctly Numbers of techniques has proposed to mitigate the effect of process and NBTI effect but have limitation. In this paper Adaptive Body Bias technique is proposed which mitigate the effect of NBTI and process variation. The simulation result shows that proposed method compensate the change in threshold voltage due to process variation/NBTI.

***Index Terms*—Adaptive Body Bias (ABB), Forward Body Bias (FBB), Intradie, Interdie, Negative Bias Temperature Instability (NBTI), Process Variation, SRAM, VLSI.**

I. INTRODUCTION

With increasing the complexity of IC's, it demands to increase the no. transistor's on the same IC i.e. the no. of transistor is being fabricated on the IC are increasing and following the Moore's law. To increase the chip density the size of the transistor has to be scale down which causes process variation. The process variation become severe as technology is scaled.Process variation occurs due to the limitation of fabrication process.Parameter variations can be considered into two broad areas as spatial and temporal.

A. Spatial Variations:

The variation in device characteristics at t = 0 s is due to spatial process variation. Such variation can be subdivided into interdie and intradie process variations. Parametric variations between dies that come from Altered runs, lots, and wafers are considered into interdie variations whereas variation of transistor strengths within the same die are defined as intradie variations. Fluctuations in length , width , flat-band conditions,oxide thickness etc., cause interdie process variations while line edge roughness (LER) or random dopant fluctuations (RDFs) give rise to intra-die random variations in process parameters [2]–[6].

B. Temporal Variations:

Until now we have discussed the impact of process Variability on the device characteristics. Due to scaled dimensions, the operating conditions of the ICs also change circuit performance. Here we describe several mechanisms responsible for temporal variations.

C. NBTI:

In particular, temporal reliability issue NBTI is the primary reliability concern for Nano-scale transistors. NBTI is a result of continuous trap generation in Si-SiO2 interface of pMOS transistors [1,5].

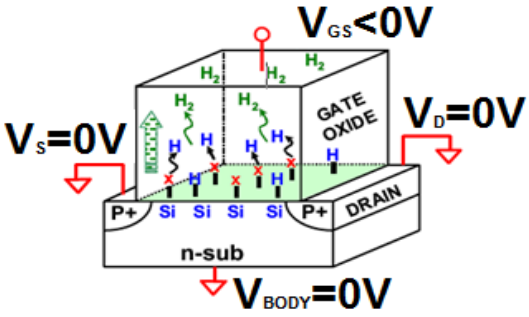

Fig. 1 NBTI Effect

In bulk-MOSFETs, dangling Si bonds exists due to structural mismatch at the Si-SiO2 interface which acts as charged interfacial traps. Usually, hydrogen passivation is applied at the silicon surface after the oxidation which converts the dangling Si atoms to Si-H atoms.However, with age and voltage stress these Si-H bonds break during the operation and again forming the interfacial traps and thereby increasing the threshold voltage of pMOS devices [6]. The interaction of inversion layer holes with hydrogen-passivated Si atoms can break the Si-H bonds, creating the interfacial traps and neutral H atoms. These H atoms can either form H2 molecules or can anneal any existing traps. NBTI is typically seen as a threshold voltage shift after a negative bias has been applied to a MOS gate at elevated temperature, mainly affecting the pMOS transistors.

II. PROPOSED ADAPTIVE BODY BIAS CIRCUIT

Lot of research has been done to overcome the effect of process variation at different level of abstraction (device / circuit /architecture. Numbers of techniques has proposed to mitigate the effect of process and NBTI effect but have limitation [3].Here we will be focus about body biasing techniques. Adaptive body bias (ABB) permits the alteration of the transistor threshold voltage by governing the transistor body-to-sourcevoltage. A forward body bias (FBB) (i.e.,V_{SB}>0) reduces threshold voltage Vt, increasing the device speed at the expense of increased leakage power. Alternatively, a reverse body bias (RBB) (i.e.,V_{SB}<0) increases, reducing the leakage power but slowing the device [4]. Therefore, the effect of process variations is mitigated by ABB circuit]. In this paper, a novel direct ABB (D-ABB) circuit is proposed.It is based on estimation circuits and direct adaptivecontrol of the body bias, accomplished by an controller circuit. This direct controller circuit produces the appropriate body bias voltage, the goal of the proposed D-ABB is to reduce the process variations impact by considering D2D and

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WID variations. This goal is achieved by using a direct controller circuit which exhibit slow area overhead compared to other ABBcircuits.

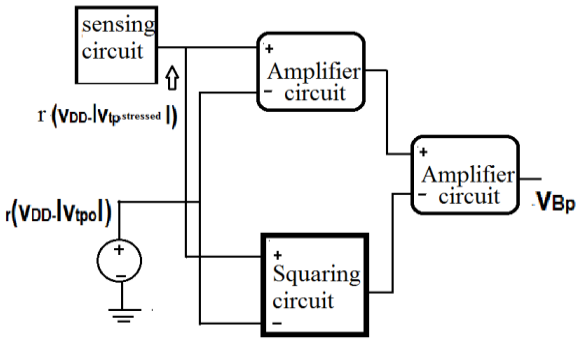

Fig.2 D-ABB circuit

In the proposed D-ABB circuit, the effect of NBTI on V_{TP} is compensated by estimating the actual value of V_{TP}, which is impacted by NBTI, by using an estimation circuit. Then, the analog controller generates the appropriate body-bias voltageV_{SB}, to mitigate the NBTI impact. The analog controller is a direct implementation of the relationship between V_{TP} and V_{SB}. In [9] and [10], the relationship between V_{TP} and V_{SB} for a pMOS transistor is given by

$$|V_{TP}| = |V_{tpo}| + \Delta|V_t|_{BB}$$

$$\text{And } \Delta|V_{tp}|_{BB} = \gamma\,[(\phi_F - V_{SB})^{1/2} - (2\phi_F)^{1/2}] \qquad (1)$$

Where $|Vtpo|$ is the pMOS transistor threshold voltage at zero body bias (i.e., when $V_{SB} = 0$), $\Delta|V_{tp}|_{BB}$ is the body-bias effect on $|V_{TP}|$, γ is the body effect coefficient, and ϕ_F is the Fermi potential with respect to the midgap in the Body. [10], if $|V_{tpo}|$ is increased due to NBTI by $\Delta|V_{tp}|_{NBTI}$. Therefore, the body-bias voltage, V_{SB}, compensates for this NBTI by producing a threshold voltage change, $\Delta|V_{tp}|_{BB}$, that terminate the NBI change, $\Delta|V_{tp}|_{NBTI}$(i.e.,$\Delta|V_{tp}|_{BB} = -\Delta|V_{tp}|_{NBTI}$). The value of V_{SB} that compensates for the NBTI change is given by Putting the value of $\Delta|V_{tp}|_{BB}$, above equation will give

$$V_{SB} = 2[(2\phi_F)^{1/2}] \times [\Delta|V_{tp}|_{NBTI} - \frac{1}{\gamma^2}(\Delta|V_{tp}|_{NBTI})^2] \qquad (2)$$

Where $|V_{tp}|_{NBTI}$ is thedifference between the estimated thresholdvoltage, which is impacted by the process variations, and the nominal threshold voltage. Typically, the source of the pMOS transistor is connected to the supply voltageV_{DD} Therefore, the body-bias voltages of the pMOS transistor, V_{BP}, which result in NBTI compensation, is given by

$$V_{BP} = V_{DD} - \frac{2[(2\phi F)^{1/2}]}{\gamma}[|V_{tpstressed}| - |V_{tpo}|] + \frac{1}{\gamma^2}[|V_{tpstressed}| - |V_{tpo}|]^2 \qquad (3)$$

The proposed D-ABB circuit is depicted in Fig. 3. For the bias voltages. A sensing circuit estimates the actual values of the threshold voltages, which are impacted by the process variations and NBTI. The sensing circuit for the pMOS transistor, shown in Fig. 3, outputs an estimate for the pMOS threshold voltage, denoted by

$$V_{out} = r\,(V_{DD} - |V_{tpstressed}|)$$

That is given to an amplifier circuit and a squaring circuit to produce the required bias voltage, which is capable of reducing the impact of NBTI. The implementations of the sensing circuit, the amplifier circuit and the squaring circuit are given in below respectively.

A. Sensing Circuit

The sensing circuit for the pMOS transistor, shown in fig.3.This is used to estimate the actual value of pMOS transistor threshold voltage. In this circuit, the pMOS transistor is sized with the same sizing as the pMOS transistor in the test circuit and then MOS transistor is a native transistor.By using the α−power law model, introduced in [11], and equating the dc currents of the nMOS and pMOS transistors,

The output voltage of Sensing circuit, Vout, is expressed as

$$V_{out} = V_{tn} + r\,(V_{DD} - |V_{tpstressed}|)$$

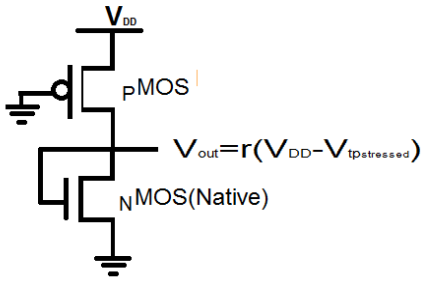

Fig. 3 $|V_{tp}|$ Sensing circuit

$$\approx r\,(VDD - |V_{tpstressed}|) \qquad (4)$$

$$\text{And } r = \left(\frac{KP\ W/L|_P}{KN\ W/L|_N}\right)^{1/\alpha}$$

Where K_N and K_P are the technological parameters, and $\frac{W}{L}|P, \frac{W}{L}|$Nare the sizes of the pMOS and the nMOS transistors, respectively. It should be noted that the native nMOS transistorthreshold voltage, V_{tn}, is assumed to be 0V in [10].

Fig. 3 displays the output voltage of the sensing circuit, Vout versus (V_{DD} − |Vtpo|).

r (V_{DD}- $|V_{tpstressed}|$) is a dc bias voltage representing the nMOS transistor nominal threshold voltage value at zero body bias.

ISSN: 2277-3754
ISO 9001:2008 Certified
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B.AmplifierCircuit

For D-ABB circuit is shown in Fig.3, several amplifiers with various gains and a large output voltage swing is required. Therefore, the two-stage configuration amplifier circuit, shown in Fig.3, is used. The advantage of this configuration is that it isolates the gain and the output voltage swing requirements. The first stage is configured in a differential pair topology to provide the high gain requirements. Naturally,the second stage is configured as a common source stage to allow maximum output voltage swings [5].Assuming that the following transistors pairs, (NM1 and NM2), (PM1 and PM2) and (NM3and NM5) are matched. According to [16], the mismatch between these transistors threshold voltages is inversely proportional to the square root of the channel area (WL).

It should be noted that the amplifier shown in Fig. 4 is work as a non-inverting amplifier.Though; this amplifier is configured as an inverting amplifier by changing the input terminals. (i.e., *V*in2 and *V*in1 become the inputs to transistors NM1 and NM2, respectively}.

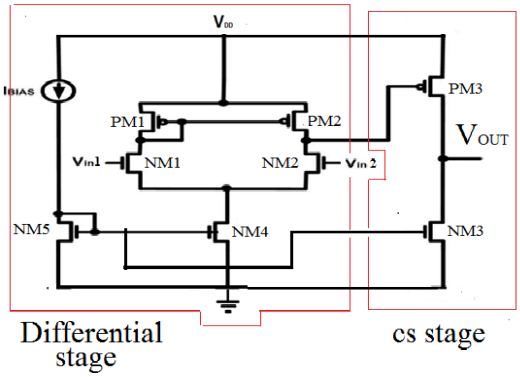

Fig.4 Proposed Amplifier Circuit

C. Squaring Circuit

One of the essential building blocks in the ABB circuit, shown in Fig. 2, is the squaring circuit. Several squaring circuits are reported in the literature [12], [13]. Fig. 5 depicts the squaring circuit used in the proposed ABB circuit. The proposed squaring circuit a utilized to adjust the squaring circuit output voltage dc offset and the squaring circuit gain.Assuming long channel transistor operation, all transistors are operating in the pinch-off saturation region, and the transistors (PM6 and PM7), (PM9, PM10), PM11, and PM12), (PM1, PM3, and PM4), (NM2 and NM3), and (NM1 and NM4), are matched.

The small signal current flowing through PM6 is $gm6Vin/2$ that is equal to the small signal current flowing through NM3,which is $gm9Vo1/2$ due to the current mirror action between these transistors.

Therefore, $Vo1 = (gm1/gm6)Vin$.

Similarly, due to the current mirror action between these transistors. Therefore, $Vo1 = (gm6/gm9)Vin$.

Similarly, due to the current mirror action between transistors NM1 and NM4, the voltage $Vo2$ is $-(gm6/gm11)$ Vin. Since transistorsMd6, PM9, PM10, PM11 and PM12 are matched, the two output voltages, $Vo1$ and $Vo2$, are given by

$$Vo1 = -Vo2 = (gm1/gm9)Vin. \quad (5)$$

These two output voltages, $Vo1$ and $Vo2$, have an equal common-mode voltage, V_{REFSQ}. When these two output voltages are applied to the basic squaring circuit, the finally output voltage, V_{outSQ}, is given by [13].

$$V_{outSQ} = V_{DD} + \frac{(V_{B+} - |V_{TP}|)^2 - (V_{REFSQ} + |V_{TP}|)^2}{2(V_{B+} - V_{REFSQ} - 2|V_{TP}|)} + \frac{(gm6/gm9)^2 \times V_{in}^2}{2(V_{B+} - V_{REFSQ} - 2|V_{TP}|)} \quad (6)$$

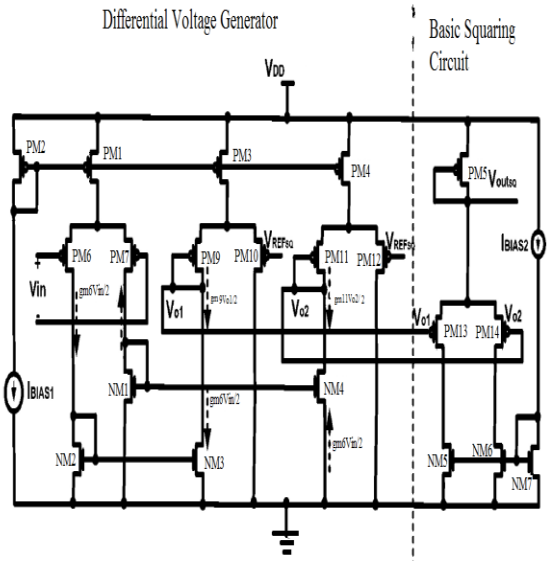

Fig.5 Squaring Circuit.

III. SIMULATION RESULT AND DISCUSSION

Tanner 14.1 tool' schematic editor is used to draw schematic and to simulate the proposed design. Schematic of the proposed ABB circuit is first designed on tanner's schematic editor and netlist of the circuit is than taken out. This netlist runs with 45 nm Predictive Technology Model (PTM) file on tanner's spice simulator to get simulation results. The simulation result of the ABB circuit shown in Table 1 shows the effectiveness of the proposed design. The circuit design, generate the body bias voltage required to compensate the effect of change in threshold voltage due to NBTI or process variations.

Sensing Circuit:

The schematic diagram of sensing circuit is given below. The effect of process variation on threshold voltage of the pMOS device is reflected by changing the threshold voltage in the ptm file. The simulation result of the sensor circuit shows a linear behavior between the threshold voltage of thep MOS and output of the sensor

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circuit i.e. the sensor circuit sense voltage values and their actual values prove that the threshold voltage sensing circuit is effective, when used in nanometer technologies.

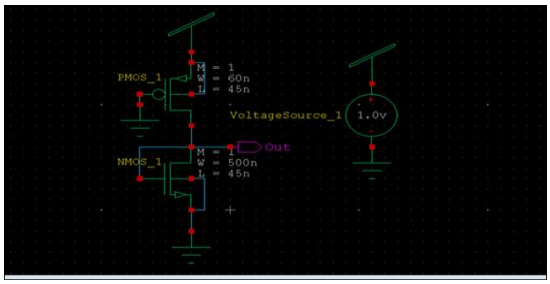

Fig.6 Schematic Diagram of Sensing Circuit

The simulation result of sensing circuit is shown in fig.7

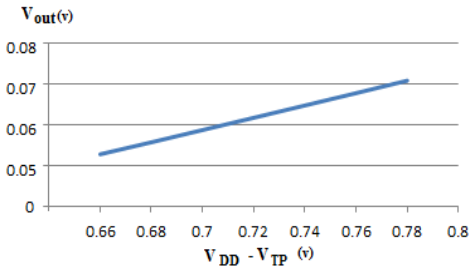

Fig.7 Output of the pMOS threshold voltage sensing circuit.

Amplifier Circuit:

The simulation result of the amplifier circuit shows linear property in a particular range. We are biasing the circuit in in this linear rang to get ideal characteristics. The gain of proposed amplifier is A = 15. By changing the biasing current and transistor sizing the gain of the amplifier can be modified as required.

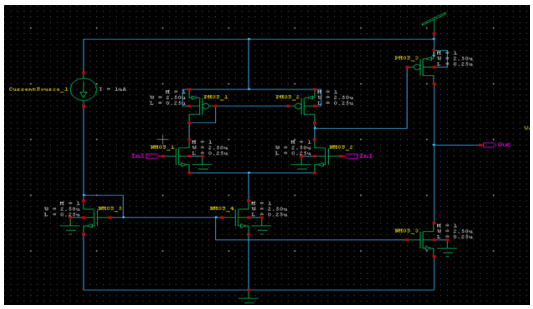

Fig.8 Schematic Diagram of Amplifier

Squaring Circuit:

The simulation result of squaring circuit is shown in fig. 9. From the fig. it can be seen that output follows the parabolic curve to satisfy the squaring equation.

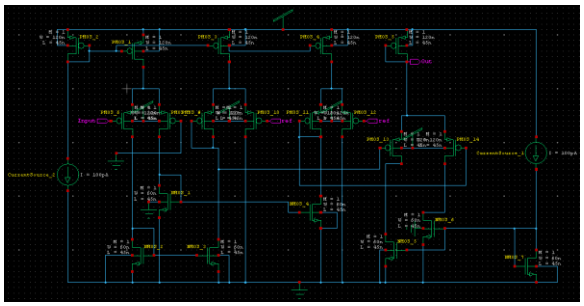

Fig.9 Schematic Diagram of Squaring Circuit

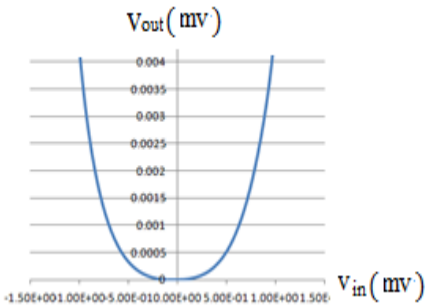

Fig.10 Output of the squaring circuit

D-ABB Circuit:

Finally all the block of the D-ABB circuit when combined produces body bias voltage (V_{BB}) according to nullify the effect of process variation.

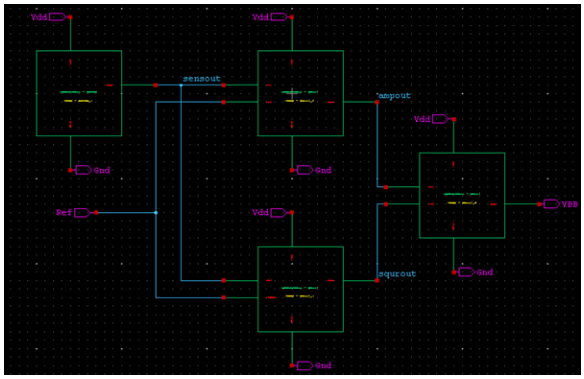

Fig.11 Schematic Diagram of D-ABB Circuit

Table 1: Simulation Results of VBB for Different V_{th} by Sensing Circuit.

V_{tp} of senser circuit (v)	V_{BB} of ABB circuit (mv)
0.22	0.76465
0.23	0.58551
0.24	0.45184
0.25	0..35231
0.26	0.27834
0.27	0.22346
0.28	0.18281
0.29	0.15274
0.30	0.13053

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IV. CONCLUSION

In this paper we have implemented adaptive body bias technique to mitigate the effect of NBTI and process variation. The simulation result shows that proposed method compensate the change in threshold voltage due to process variation/NBTI. The proposed technique alleviates effect of process and NBTI at run time with small area overhead compared to the existing techniques.

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