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An Improved Transformerless Inverter For Grid-Connected Photovoltaic Power Systems

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Abstract*— The traditional grid-connected PV inverter includes either a line frequency or a high frequency transformer between the inverter and grid. The transformer provides galvanic isolation between the grid and the PV panels. In order to increase the efficiency, to reduce the size and cost, the effective solution is to remove the isolation transformer. It leads to appearance of common mode (CM) ground leakage current due to parasitic capacitance between the PV panels and the ground. The common mode current reduces the efficiency of power conversion stage, affects the quality of grid current, deteriorate the electric magnetic compatibility and give rise to the safety threats. In order to eliminate the common mode leakage current in transformerless PV system, the concept of virtual DC bus is proposed in this project. By connecting the grid neutral line directly to the negative pole of the DC bus, the stray capacitance between the PV panels and the ground is bypassed. The CM ground leakage current can be suppressed completely. Virtual DC bus is created to provide the negative voltage level for the negative AC grid current generation. The virtual DC bus is realized with the switched capacitor technology that uses less number of elements. Therefore, the power electronic cost can be reduced. This topology can be modulated with the unipolar SPWM to reduce the output current ripple. A smaller filter inductor can be used to reduce the size and magnetic losses. The simulation result of the proposed topology using MATLAB/SIMULINK is presented.

***Index Terms*— Common Mode Leakage Current, Transformerless Inverter, Unipolar SPWM.**

I. INTRODUCTION

Renewable energy sources become a more and more important contribution to the total energy production in the world. Today the energy production from solar energy compared to the other renewable energy sources is very low, but the PV systems are one of the fastest growing in the world. The price of PV system components, especially the PV modules are decreasing and the market for PV is expanding rapidly. Solar power will be dominant because of its availability and reliability. Photovoltaic inverters become more and more widespread within both private and commercial circles. These grid-connected inverters convert the available direct current supplied by the PV panels and feed it into the utility grid. According to the latest report on installed PV power, during 2012, there has been a total of 69.3 GW of installed PV systems in the world out of which the majority (35.8%) has been installed in Germany. India has installed 427 MW solar power which is 0.6% of total installed power in the world. At the end of 2012, the total installed PV capacity will reach 80.0 GW of which around 90% is grid connected. There are two main inverter topologies used in the case of grid-connected PV systems, namely, with and without galvanic isolation. Galvanic isolation can be on the dc side in the form of a high-frequency dc–dc transformer or on the grid side in the form of a big bulky ac transformer. Both of these solutions offer the safety and advantage of galvanic isolation, but the efficiency of the whole system is decreased due to power losses in these extra components. In case the transformer is omitted, the efficiency of the whole PV system can be increased with an extra 1%–2%. The most important advantages of transformerless PV systems can be observed in Fig.1, such as higher efficiency and smaller size and weight compared to the PV systems that have galvanic isolation (either on the dc or ac side). Fig.1 has been made from the database of more than 400 commercially available PV inverters, presented in a commercial magazine about PV systems [1]. The efficiency of commercial PV panels is around 15-20%. Therefore, it is very important that the power produced by these panels is not wasted, by using inefficient power electronics systems. The efficiency and reliability of both single-phase and three phase PV inverter systems can be improved using transformerless topologies, but new problems related to leakage current and safety need to be dealt with. The size and cost of the inverter need to be reduced.

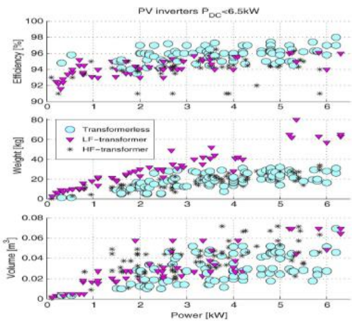

Fig 1. Advantages And Drawback Of Different Inverter Topologies

The efficiency of commercial PV panels is around 15-20%. Therefore, it is very important that the power produced by these panels is not wasted, by using inefficient power electronics systems. The efficiency and reliability of both single-phase and three phase PV inverter systems can be

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improved using transformerless topologies, but new problems related to leakage current and safety need to be dealt with. The size and cost of the inverter need to be reduced. The main goal of this project is to analyze and model transformerless PV inverter systems with respect to the leakage current phenomenon that can damage the solar panels and pose safety problems. New topologies and control strategies that will minimize the leakage current, reduce the size, cost and exhibit a high efficiency is proposed, and verified.

II. REVIEW OF EXISTING INVERTER TOPOLOGIES

A. *Common Mode Current*

If the transformer is omitted, the common mode (CM) ground leakage current may appear on the parasitic capacitor between the PV panels and the ground [2] [3]. The existence of the CM current may reduce the power conversion efficiency, increase the grid current distortion, deteriorate the electric magnetic compatibility, and more importantly, give rise to the safety threats [4]. The CM current path in the grid-connected transformerless PV inverter system is illustrated in Fig.2. It is formed by the power switches, filters, ground impedance Z_G and the parasitic capacitance C_{PV} between the PV panels and the ground. According to [5], the CM current path is equivalent to an *LC* resonant circuit in series with the CM voltage, as shown in Fig.3. The CM voltage v_{CM} is defined by

$$v_{CM} = \frac{v_{AO}+v_{BO}}{2} + (v_{AO} - v_{BO})\frac{L2-L1}{2(L1+L2)} \quad (1)$$

where v_{AO} is the voltage difference between point A and O, v_{BO} is the voltage difference between point B and O, and L_1 and L_2 are the output filter inductors. If the switching action of the inverter generates high frequency CM voltage, the CM current i_{CM} may be exited on the *LC* circuit. From this point of view, the topology and modulation strategy adopted for the transformerless PV power system should guarantee that v_{CM} is constant or only varies at low frequency, such as 50Hz/60Hz line frequency.

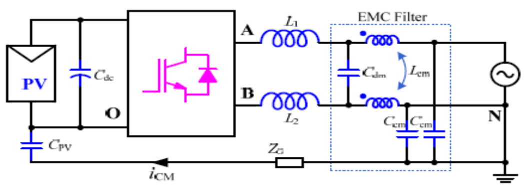

Fig 2. CM Current Path For Transformerless PV Inverter

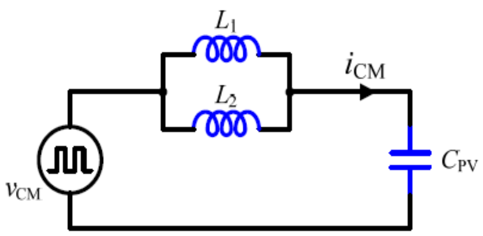

Fig 3. Equivalent circuit fr Current path

B. *State-of-the-art Topologies*

One of the way to realize this goal is to use full bridge inverter with the bipolar sinusoidal pulse width modulation (SPWM). Though the unipolar SPWM has better performance when compared to bipolar SPWM, it cannot be used directly for the full bridge inverter because it generates switching frequency CM voltage. For this reason, some of the topologies based on the full bridge inverter with unipolar SPWM such as the H5 inverter, the HERIC inverter, H6 inverter with AC bypass and H6 inverter with DC bypass have been developed. Such inverter topologies require two filter inductors which may lead to a rise in the size and cost. The DC and AC sides cannot be perfectly disconnected by the power switches because of the switch parasitic capacitance, so the common mode current may still exist [5]. If half bridge inverter topologies are used such as conventional half bridge inverter and neutral point clamped (NPC) half bridge inverter, then the required DC bus voltage should be doubled compared with the full bridge topologies. Beside the classic circuits above, there are other topologies proposed in recent literatures. The Karschny inverter [6] and the paralleled-buck inverter [7] are derived from the buck-boost and buck circuits respectively. These solutions have high reliability, but are not capable of supplying the reactive power to the grid. The inverter proposed in [8] employs a capacitor voltage divider to keep the CM voltage constant, but is regarded to be of higher conduction losses.

III. NEGATIVE VOLTAGE GENERATION

The concept of the negative voltage generation is depicted in Figure.4. By connecting the grid neutral line directly to the negative pole of the PV panel, the voltage across the parasitic capacitance C_{PV} is clamped to zero. This prevents any leakage current flowing through it. With respect to the ground point N, the voltage at midpoint B is either zero or $+V_{dc}$, according to the state of the switch bridge. The purpose of introducing virtual DC bus is to generate the negative output voltage, which is necessary for the operation of the inverter. If a proper method is designed to transfer the energy between the real bus and the virtual bus, the voltage across the virtual bus can be kept the same as the real one. As shown in Fig.4, the positive pole of the virtual bus is connected to the ground point N, so that the voltage at the midpoint C is either zero or $-V_{dc}$. The dotted line in the figure indicates that this connection may be realized directly by a wire or indirectly by a power switch. With points B and C joined together by a smart selecting switch, the voltage at point A can be of three different voltage levels, namely $+V_{dc}$, zero and $-V_{dc}$. Since the CM current is eliminated naturally by the structure of the circuit, there's not any limitation on the modulation strategy, which means that the advanced modulation technologies such as the unipolar SPWM or the double frequency SPWM can be used to satisfy various PV applications.

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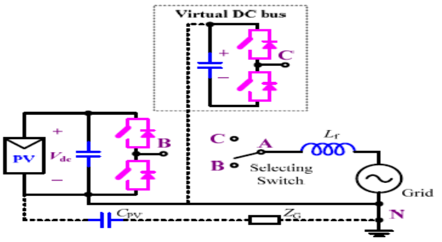


Fig 4. Negative Voltage Generation

III. PROPOSED TOPOLOGY AND MODULATION

Based on the negative voltage generation concept, an inverter topology is derived to show the clear advantages of the proposed methodology, which is shown in Fig.5. It consists of five power switches S_1~S_5 and only one single filter inductor L_f. The PV panels and capacitor C_1 form the real DC bus while the virtual DC bus is provided by C_2. With the switched capacitor technology, C_2 is charged by the real DC bus through S_1 and S_3 to maintain a constant voltage. This topology can be modulated with the unipolar SPWM and double frequency SPWM. The detailed analysis is introduced as follows.

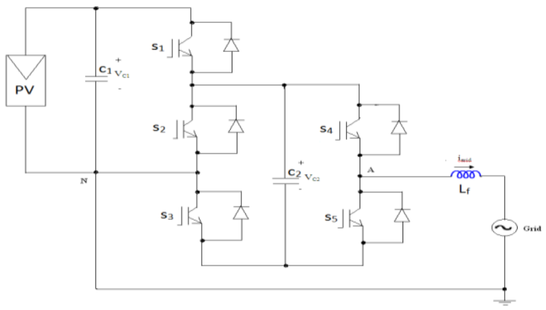


Fig 5. Proposed Topology

A. *Unipolar SPWM*

The waveform for the unipolar SPWM of the proposed inverter is displayed in Fig.6. The gate drive signals for the power switches are generated according to the relative value of the modulation wave *ug* and the carrier wave u_c. During the positive half grid cycle, $u_g > 0$. S_1 and S_3 are turned on and S_2 is turned off, while S_4 and S_5 commutate complementally with the carrier frequency. The capacitors C_1 and C_2 are in parallel and the circuit rotates between state 1 and state 2 as shown in Fig.7. During the negative half cycle, $u_g < 0$. S_5 is turned on and S_4 is turned off. S_1 and S_3 commutate with the carrier frequency synchronously and S_2 commutates in complement to them. The circuit rotates between state 3 and state 2. At state 3, S_1 and S_3 are turned off while S_2 is turned on. The negative voltage is generated by the virtual DC bus C_2 and the inverter output is at negative voltage level. At state 2, S_1 and S_3 are turned on while S_2 is turned off. The inverter output voltage v_{AN} equals zero, meanwhile C_2 is charged by the DC bus through S_1 and S_3.

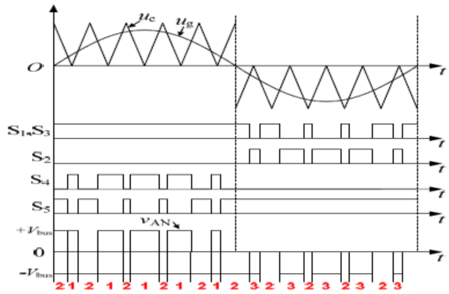
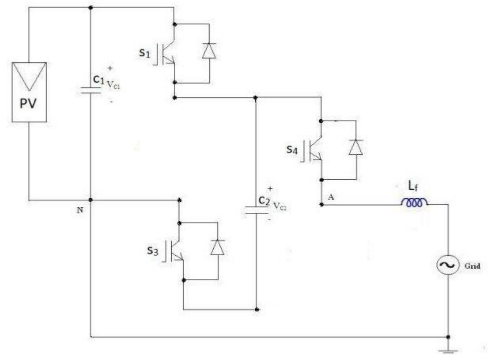


Fig 6. Unipolar SPWM For Proposed Topology

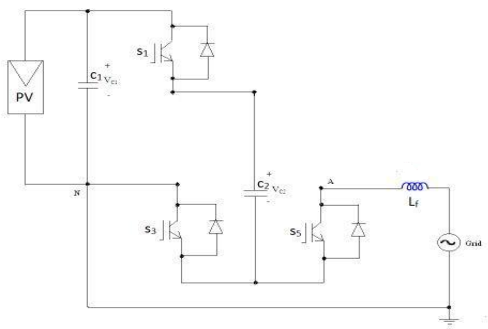
The summary of operation state of the switches for proposed topology is shown in Table 1.

TABLE I. SUMMARY OF OPERATION OF SWITCHES

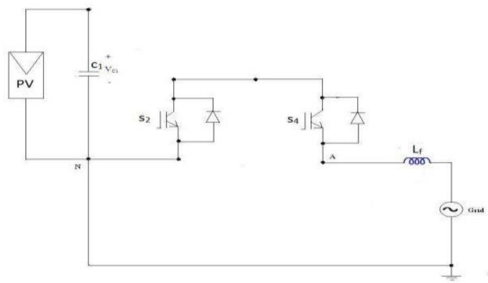
STATE	SWITCHES				
	S_1	S_2	S_3	S_4	S_5
1	ON	OFF	ON	ON	OFF
2	ON	OFF	ON	OFF	ON
3	OFF	ON	OFF	OFF	ON
4	OFF	ON	OFF	ON	OFF



(a)



(b)



(c)

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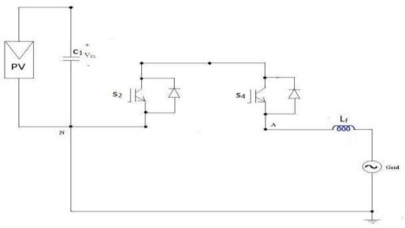

(d)

Fig 7. Operation States Of Proposed Topology : (A) State 1; (B) State 2; (C) State 3; (D) State 4

IV. MATLAB / SIMULINK MODEL

A. The Fig.8 shows the MATLAB / Simulink model for proposed inverter topology.

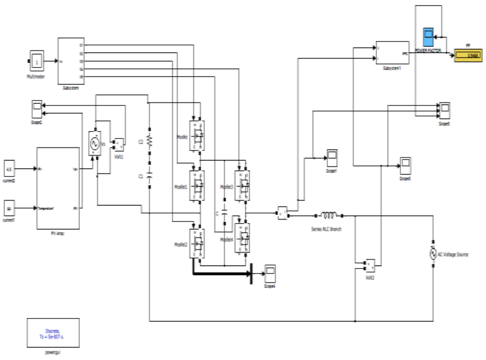

Fig 8. Simulink Model For Proposed Topology

The Fig.9 shows the MATLAB / Simulink model for solar PV cell.

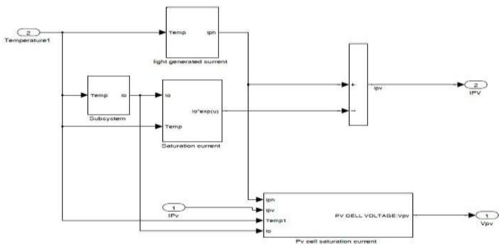

Fig 9. Simulink Model For Solar PV Cell

The Fig.10 shows the MATLAB / Simulink model for solar PV cell.

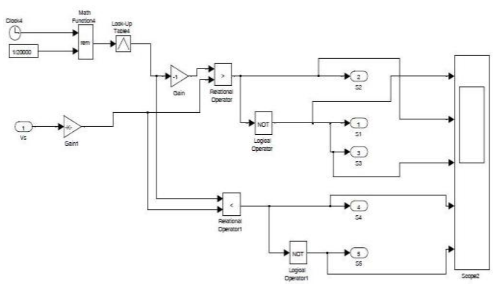

Fig 10. Simulink model for unipolar SPWM

The Fig.11 Shows The Output Voltage Of Grid. The Value Of Grid Voltage Is 340V AC.

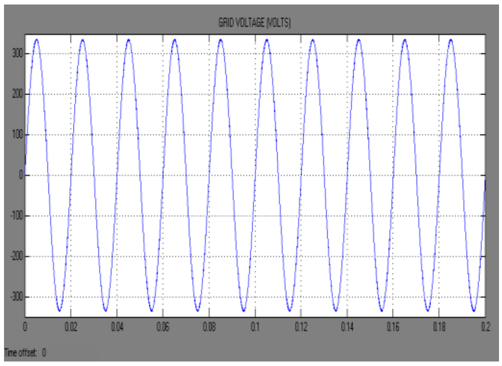

Fig 11. Waveform Of Grid Voltage

The Fig.12 Shows The Output Current Of Proposed Inverter. The Value Of Current is 2.9 A.

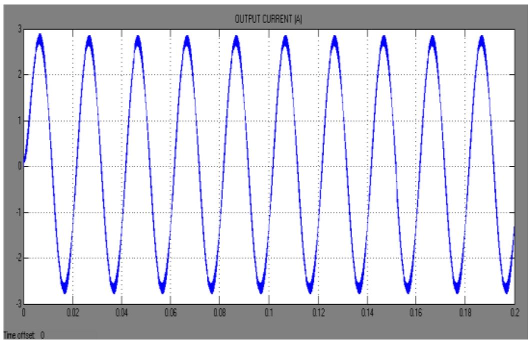

Fig 12. Waveform Of Inverter Output Current

V. CONCLUSION

The concept of the virtual DC bus is proposed to solve the CM current problem for the transformerless grid-connected PV inverter. By connecting the negative pole of the DC bus directly to the grid neutral line, the voltage on the stray PV capacitor is clamped to zero. This eliminates the CM current completely. Meanwhile, a virtual DC bus is created to provide the negative voltage level. The required DC voltage is only half of the half bridge solution, while the performance in eliminating the CM current is better than the full bridge based inverters. Based on this idea, a novel inverter topology is proposed with the virtual DC bus concept by adopting the switched capacitor technology. It consists of only five power switches and a single filter inductor. The proposed topology is especially suitable for the small power single phase applications, where the output current is relatively small so that the extra current stress caused by the switched capacitor does not cause serious reliability problem for the power devices and capacitors. With excellent performance in eliminating the CM current, the virtual DC bus concept provides a promising solution for the transformerless grid-connected PV inverters. The software tool used in this project is MATLAB 2011b.

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