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Analysis and Study of FGMOS Based Current Mirror Circuit Using 0.35µm Technology

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Abstract: ***Analysis of Floating Gate MOSFETs (FGMOS) is carried out. Circuits like simple current mirror and FGMOS based current mirror are discussed. FGMOS based current mirrors can be operated at lower voltage levels. FGMOS based cascode current mirror circuit is also simulated. Parameters like current range, voltage requirements, Bandwidth and region of operation are checked. Simulation has been carried out using Tanner EDA for 0.35 nm TSMC technology.***

Index Terms**— FGMOS, Current Mirrors, Low Voltage, Low Power**

I. INTRODUCTION

The fast development of electronic-based entertainment, computing and communication tools, especially portable ones, has provided a strong technology drive for microelectronics. System portability usually requires battery supply and therefore weight/energy storage considerations. Unfortunately, battery technologies do not evolve as fast as the applications demand. Therefore the challenge, derived from market requirements, is to reduce the power consumption of the circuit. [1] FGMOS based current mirror offer improved linear relationship of reference current with output current.

II. FLOATING GATE MOSFET (FGMOS)

An FGMOS can be fabricated by electrically isolating the gate of a standard MOS transistor, so that there are no resistive connections to its gate. A number of secondary gates or inputs are then deposited above the floating gate (FG) and are electrically isolated from it. These inputs are only capacitively connected to the FG, since the FG is completely surrounded by highly resistive material. So, in terms of its DC operating point, the FG is a floating node.[1] FGMOS based circuits can operate at power supply voltage levels which are well below the intended operational limits for a particular technology and consume less power than the minimum required power of a circuit designed with only MOS devices in the same technology with the same performance. [2-5] whilst a conventional MOS transistor has only one input, FGMOS has several. By using FGMOS in right way- establishing appropriate relationship between its inputs- it is possible to design trade-offs that are not possible with conventional MOS devices. Figure.1 shows that the Floating Gate can be fabricated using the gate electrode (poly1) layer, extends outside the active area of the MOS transistor. The FG is surrounded by two SiO2 insulator layers and thus electrically isolated from the rest of the device.

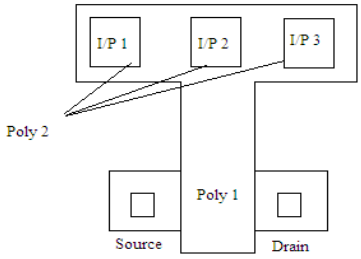

Fig-1 FGMOS Fabrication [1]

Multiple-input floating-gate (MIFG) transistor with n-inputs can be represented as shown in figure 2(a) along with its equivalent circuit, shown in figure 2 (b). The floating-gate (FG) of the structure is capacitively coupled to the input gates and the voltage present at this gate can modulate the channel current. [6]

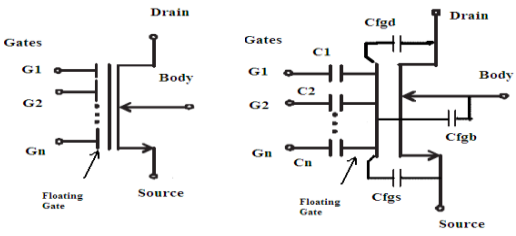

Fig-2(a) **Fig-2 (b)**

Fig-2 (a) Symbol of MIFG transistor (b) Equivalent circuit [6]

Gate (G1) is used for signal input gate and Gate (G2) is used for biasing.

Considering Vs=V_B=0, V_{fg} is given by,

$$V_{fg} = \frac{C_1}{C_{Total}}V_1 + \frac{C_2}{C_{Total}}V_2 + \frac{C_{fgd}}{C_{Total}}V_{DS} \quad \text{.....(1)}$$

Keeping C_1, C_2>>C_D,

The drain current (I_D) of the FGMOS when operating in ohmic region is given by:

$$I_D = \beta\left[\left\{\left(\frac{C_1}{C_{Total}}V_1 + \frac{C_2}{C_{Total}}V_2\right) - V_T\right\} - \frac{V_{DS}}{2}\right]V_{DS} \quad \text{.....(2)}$$

Where β is Tran conductance parameter given by,

$$\beta = \mu_n C_{ox}\frac{W}{L} \quad \text{.....(3)}$$

Total floating-gate (FG) capacitance, given by $C_{Total} = C_1 + C_2$

V_T is the threshold voltage. Equation (2) may be simplified as

$$I_D = \beta\left(\frac{C_1}{C_{Total}}\right)\left[\left(V_1 - V_{T,eff}\cdot\right)V_{DS} - \frac{C_{Total}}{2C_1}V_{DS}^2\right] \quad \text{.....(4)}$$

Where effective threshold voltage ($V_{T,eff}$) is given by:

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$$V_{T,eff.} = V_T + \frac{C_2}{C_1}(V_T - V_2) \quad \text{.....(5)}$$

Thus, the reduction in VT,eff can be done by selecting $V_2 > V_T$ and $C_2 > C_1$.

For saturation region, drain current I_D is given by, [6]

$$I_D = \frac{\beta}{2}(V_{FG} - V_T)^2 \quad \text{..... (6)}$$

$$I_D = \frac{\beta}{2}\left[\left(\frac{C_1}{C_{Total}}V_1 + \frac{C_2}{C_{Total}}V_2\right) - V_T\right]^2 \quad \text{..... (7)}$$

Equation (7) can be written as, [7]

$$I_D = \frac{\beta}{2}k_1^2\left[V_1 - \left(\frac{V_T - k_2V_2}{k_1}\right)\right]^2 \quad \text{..... (8)}$$

$$I_D = \frac{\beta}{2}k_1^2\left[V_1 - V_{Teff}\right]^2 \quad \text{..... (9)}$$

Where, V_{Teff} is given by,

$$V_{Teff} = \frac{(V_T - V_2k_2)}{k_1} \quad \text{..... (10)}$$

As well as, k1 and k2 are given by,

$$k_1 = \frac{C_1}{C_{Total}} \text{ and } k_2 = \frac{C_2}{C_{Total}} \quad \text{..... (11)}$$

So, by changing the bias voltage, effective threshold can be reduced.

Pspice simulation of FGMOS

Here the simulation of FGMOS is carried out using Tanner EDA (S-Edit) for 0.35µm tsmc technology. As, Tanner does not support floating gate, resistances are connected in parallel with each capacitors. These resistors selected are of very high values in Giga ohms and capacitors selected are in femto farad range. The full model of FGMOS [6] is as shown in figure-3.

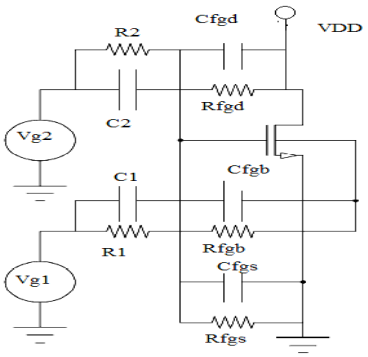

Fig 3 Pspice full model of FGMOS[6]

Considering only C1 and C2 as as effective capacitances, the full model can be reduced the model as shown in figure-4.

A two-input FGMOS, shown in Figure 4, is simulated by choosing C1=100 fF, R1= 200Ω, C2= 200fF, R2 = 100GΩ and W/L = 50µm/1µm using supply voltage of ±0.750 V. The technology used here is 0.35µm CMOS TSMC.

The transfer characteristics for different values of input signals and the drain characteristics are shown in Figures 5 and 6 respectively.

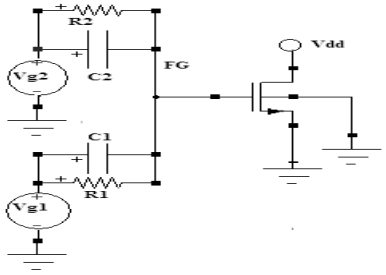

Fig-4 Compact Pspice model for 2-input FGMOS

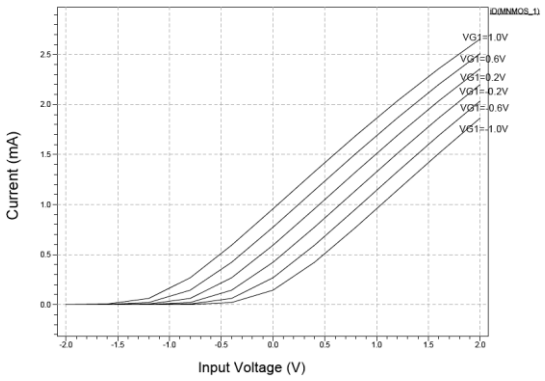

Fig-5 FGMOS transfer characteristics

Due to the presence of voltage at Floating Gate (V_{bias}) even in the absence of input signal, we get different characteristics.

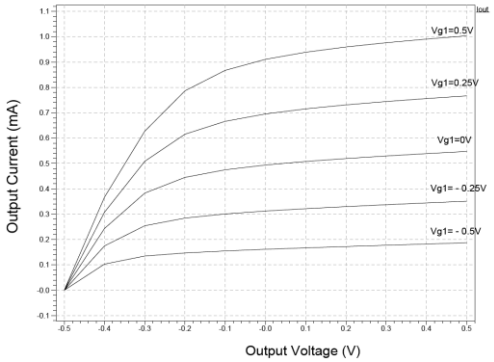

Fig-6 Drain characteristics of FGMOS

As compared to nomal MOS, here in FGMOS threshold voltages can be varied. Thus, It can be said that FGMOS and related circuits can be operated at very low voltages.

III. BASIC CURRENT MIRROR

The simple current mirror (CM) shown in figure-7 constitutes one of the simplest yet most important design blocks for analog circuit engineering. It can be used to copy reference currents or set operating points across the integrated analog circuit blocks. A current flows through M1 corresponding to V_{GS1}. Since $V_{GS1} = V_{GS2}$, ideally the same current, or a multiple of the current in M1, flows through M2. If the MOSFETs are of the same size, the same drain current flows in each MOSFET provided M2 stays in the saturation region [8].

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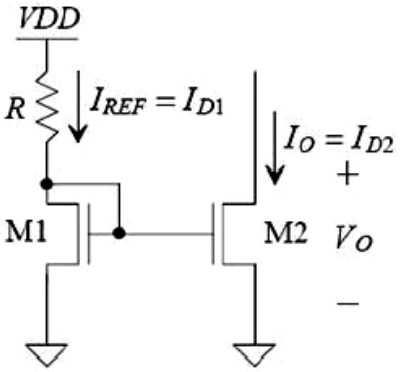

Fig-7 Basic Current Mirror

The current through M1 can be given by,

$$I_{D1} = \frac{\beta 1}{2}(V_{GS1} - V_{THN})^2 \quad \text{.....(12)}$$

And current through M2 is,

$$I_{D2} = I_o = \frac{\beta 2}{2}(V_{GS2} - V_{THN})^2 \quad \text{.....(13)}$$

Taking ratio of both currents,

$$\frac{I_{D2}}{I_{D1}} = \frac{\beta_2}{\beta_1} = \frac{W_2}{L_2} \Big/ \frac{W_1}{L_1} \quad \text{..... (14)}$$

From equation (14) we can say that the desired output current can be obtained by adjusting W/L ratios of two devices.[8]

Here it is required that M2 remains in saturation. Therefore the minimum output voltage across the current mirror is given by $V_{min}=V_{DS(SAT)}=V_{GS}-V_{THN}$ which is somewhat larger for low voltage applications. To overcome this problem, FGMOS based current mirror is introduced.

Current mirror using FGMOS

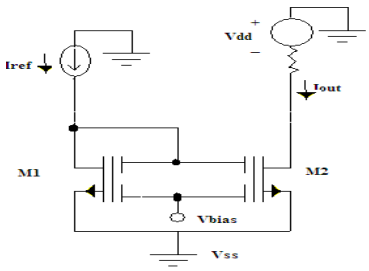

Fig-8 Current mirror using FGMOS

In low voltage design, performance of current mirror can be enhanced by programming its threshold voltage [5]. The structure of FGMOS based current mirror is shown in Figure 8 [5, 7]. This current mirror uses two-input FGMOS where one of the gate input terminals is used to program the threshold voltage of the MOSFETs using a bias voltage (V_{bias}) and the second input terminal is used for signal processing.[8] FGMOS based current mirror is simulated with tanner EDA, carried out by choosing aspect ratio (W/L) of transistors M1 and M2 as 50 µm/1 µm at a supply voltage of ±0.75V. Input voltage (V_{in}) requirement varies with input current (Iin) at different V_{bias} as shown in Figure 9.

So, it can be concluded that FGMOS based current mirror provides programmability of threshold voltage hence effective input voltage requirement can be reduced.

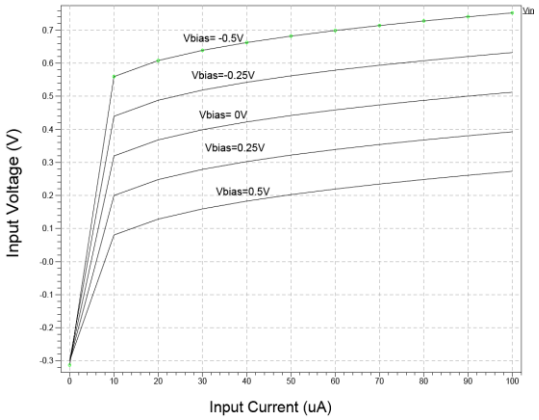

Fig-9 Variation of V_{in} with I_{in} at different V_{bias}.

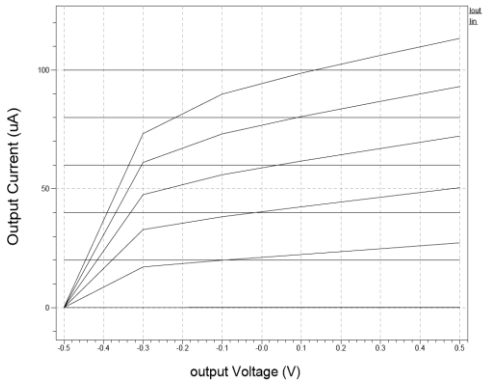

Fig-10 I-V characteristics of FGMOS based CM

Figure-10 shows output current characteristics for FGMOS based simple current mirror. The performance of FGMOS based simple current mirror is somewhat poor, here there is larger mismatch between input and output currents as shown in figure-10. The frequency response of this current mirror is shown in figure-11.

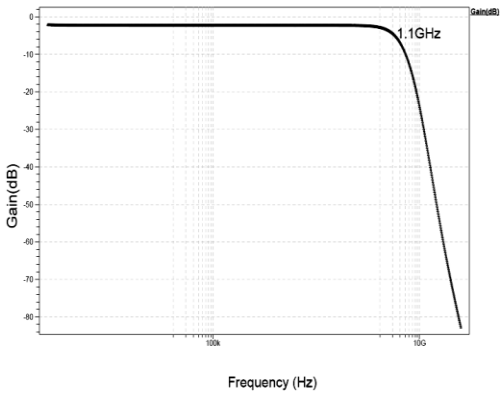

Fig-11 Frequency Response of Basic Current Mirror Using FGMOS

This mirror gives bandwidth of 1.1GHz at 500uA input current. Input voltage requirement for FGMOS based current mirror decreases because threshold voltage can be changed and can be brought to lower value. Comparison of input voltage requirement for FGMOS based basic current mirror and basic current mirror is shown in figure-12. This figure clearly shows the difference and it clarifies that FGMOS

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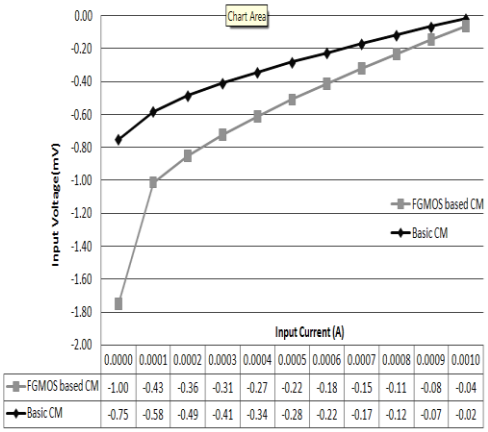
based current mirror requires less input voltage.



	0.0000	0.0001	0.0002	0.0003	0.0004	0.0005	0.0006	0.0007	0.0008	0.0009	0.0010
FGMOS based CM	-1.00	-0.43	-0.36	-0.31	-0.27	-0.22	-0.18	-0.15	-0.11	-0.08	-0.04
Basic CM	-0.75	-0.58	-0.49	-0.41	-0.34	-0.28	-0.22	-0.17	-0.12	-0.07	-0.02

Fig-12 Comparison between FGMOS Based Current Mirror and Basic Current Mirror

IV. CASCODE CURRENT MIRROR

A low voltage Cascode Current Mirror based on FGMOS is shown in Figure 13. Here M1, M2, M3 and M4 are two input FGMOS. In these MOSFET's, one gate terminal is used as normal input terminal and a biasing voltage is applied at the second gate terminal to form the conduction channel between source and drain terminals. If $(W/L)_2/(W/L)_1 = (W/L)_4/(W/L)_3$, then, $V_{GS2} = V_{GS1}$ and hence $V_X = V_Y$. This forces same current in both the branches and I_{out} becomes equal to I_{in}. Also, in this circuit all the MOSFET's are working in saturation region.

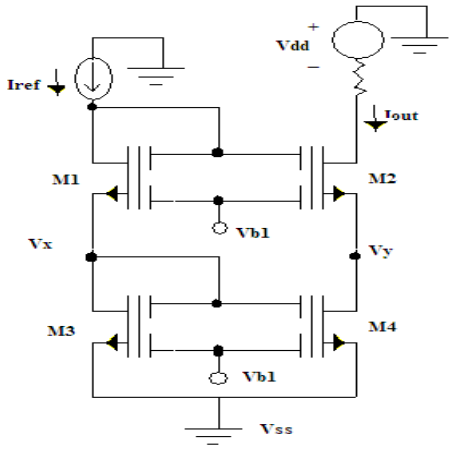


Fig-13 Cascade Current Mirror using FGMOS

Figure-14 shows the I-V characteristics of this cascode current mirror using FGMOS. As seen from the characteristics output current Iout follows Iin almost perfectly. Figure-15 clearly shows that the range of this current mirror is about 500uA. In addition to this, FGMOS based cascode current mirror provides high output impedance and low input impedance as compared to basic current mirror but the disadvantage is of poor frequency response as shown in figure-16. The bandwidth offered by this circuit is reduced to 465 MHz at 500uA input current.

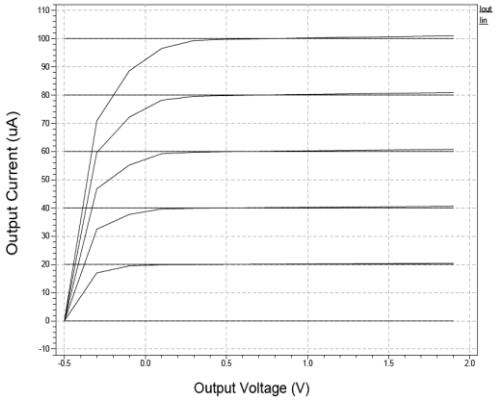


Fig-14 I-V Characteristics of FGMOS based cascode current mirror

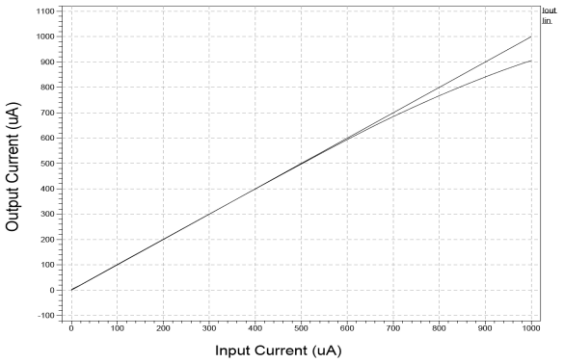


Fig-15 Simulation of FGMOS based cascode current mirror

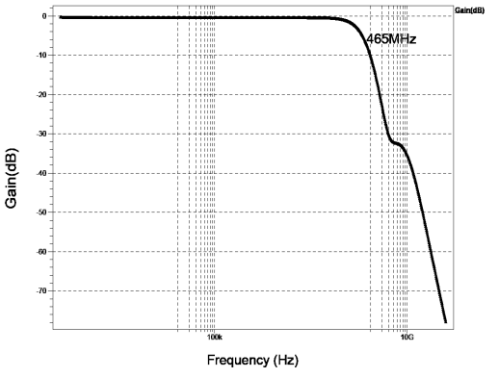


Fig-16 Frequency response of cascode current mirror using FGMOS

V. SIMULATION RESULTS

Comparison between various current mirrors

Parameters	Simple Current Mirror	FGMOS Based Current Mirror	Simple Cascode Current Mirror	FGMOS based Cascode Current Mirror
Range	0-1000µA	0-350µA	0-700µA	0-500µA
Band-width	2.58GHz	1.1GHz	1.32GHz	465MHz
Voltage	±1.0V	±0.75V	±1.0V	±0.75V
Region of Operation	Saturation	Saturation	Saturation	Saturation

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VI. CONCLUSION

In this paper, Behavior and characteristics of Floating Gate MOSFET (FGMOS) have been presented. Controlling of threshold voltage by changing bias voltage is shown. FGMOS based current mirror is compared with basic current mirror. Basic cascode current mirror and FGMOS based cascode current mirror are also analyzed. Basic Current mirror circuits operate with a supply voltage of ±1.0 V whereas FGMOS based current mirror circuits operate with supply voltage ±0.75V making them suitable for low-voltage applications.

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