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Design and Verification of Low Power 64bit SRAM System using 8T SRAM:Back-End Approach

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Abstract*— Power dissipation is one of the major concerns of Very Large Scale Integration (VLSI) circuit designs, for which CMOS is the primary technology. Low power design has become the major challenge of present chip designs as leakage power has been rising with scaling of technologies. With increasing chip densities, leakage power has become dominant in memory design. To achieve low power operation we have chosen 8T SRAM cell to design 64-bit memory of 8words x 8bits. This work targets reduction of power dissipation in SRAM system during both active and idle mode of operations. An 8T SRAM cell that uses two NMOS sleep transistors, one each in the pull down path of the two inverters of 6T SRAM cell is chosen as the ultra low power SRAM cell to build this array. This SRAM cell uses self correcting feedback to achieve stable operation. This cell also reduces dynamic power consumed during active mode of operation compared to conventional 6T SRAM cell. The functional blocks for the 64-bit memory array are 8T SRAM cell, address decoder, data write circuitry, bit line conditioning circuitry and sense amplifier. This work addresses design, simulation, and functionality verification of 8 x 8 memory array using 8T SRAM cell. Cadence Virtuoso Schematic Editor is used for circuit design and the circuit is analyzed and verified for functionality through simulations using Cadence Virtuoso Spectre tool. The static power and dynamic power measurement is done using Cadence Virtuoso ADE Visualization and Analysis XL Browser and XL Calculator. The layout is drawn and verified for DRC, LVS and RC extraction using Cadence Assura Tool. Power reduction is achieved at lower access time but with associated area overhead. The total power dissipation is lower by 3.4X as compared to standard 6T SRAM cell. The static power dissipation is lower by 16X as compared to 6T SRAM cell. The access time for write and read operations is also improved as compared to 6T SRAM System with excellent data stability.

***Index Terms*— Access Time, Static Power, Static Random Access Memory (SRAM), Total Power.**

I. INTRODUCTION

According to ITRS roadmap in 2002, memory chip will occupy 90% of chip area in 2013 [1]. Recent surveys in this area show, roughly around 30% of the semiconductor business (world-wide) are due to semiconductor memory chips. In recent years as the need of leakage reduction in general-purpose processors, microcontrollers, memory structures and SOCs increases, there have been many research activities on low-voltage SRAM dynamic and standby techniques. The power dissipation consists of dynamic and static power. Dynamic power consumption was previously the single largest concern for low-power chip designers since dynamic power accounted for 90% or more of the total chip power. However, as the feature size shrinks, static power has become a great challenge for current and future technologies. Most of the researchers reported circuit techniques in this area focusing on the designs at the sleep mode, e.g., an array of dynamically-controlled sleep transistors was used to provide a finely programmable standby VDD [2], [3]. The rising demand for multimedia rich applications in handheld devices continues to drive the need for large and high speed SRAM (Static Random Access Memory) to enhance the system performance [4]. The power sensitive portable devices need to reduce the dynamic and standby power consumption in order to meet the battery life time. Since rest of the processor has been greatly optimized to reduce the power consumption, leakage power in the CPU is mainly dominated by the large on die SRAMs. In this work an attempt has been made to reduce leakage power in SRAM using additional transistors.

A. MEMORY ARRAY ARCHITECTURE USING 8T SRAM CELL

The preferred memory system for Random access memories [5] is shown in Fig. 1. The memory locations (addresses) can be accessed in random order at a fixed rate, independent of physical location, for reading or writing. The storage array, or core, is made up of simple cell circuits arranged to share connections in horizontal rows and vertical Columns.

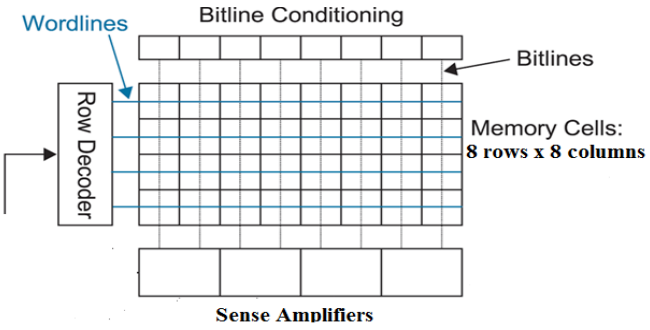

Fig. 1: Memory Array Architecture

The horizontal lines, which are driven only from outside the storage array, are called word-lines, while the vertical lines, along which data flow into and out of cells, are called bit-lines. A cell is accessed for reading or writing by selecting its row and column. Each cell can store a single bit, either '0' or '1'.

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B. Ultra Low Power 8T SRAM Cell

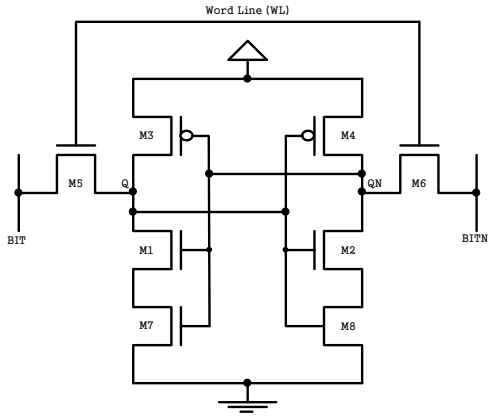

Fig. 2: 8T SRAM cell

The 8T SRAM cell consists of two cross-coupled inverters made up of transistors M1, M3 and M2, M4 [6]. The transistors M5, M6 are access transistors. The two additional NMOS transistors M7 and M8, one each in pull down path of cross coupled inverters are used to achieve leakage power reduction. The access transistors are connected to the word line at their respective gate terminals, and the bit-lines at their drain terminals. The word line is used to select the cell while the bit lines are used to perform write and read operations on the cell. Internally, the cell holds the stored value on one node and its complement on the other node. The node Q holds the stored value while other node QN holds its complement. The two complementary bit lines are used to improve speed of write and read operations. The 8T SRAM cell is shown in Fig. 2. The SRAM cell is symmetric and hence M1=M2, M3=M4, M5=M6, and M7=M8. The memory system for read and write operation [5], is given in Section II .B.

C.SRAM Memory System for Writing and Reading Single Bit Data

The Precharge Circuit [11] is used to precharge the bit-lines, BIT and BITN, to logic '1' value during inactive state of memory cell. When memory cell is being written/ read, precharging is deactivated. The *Data Write Circuit* [10] is used to write data and its complement onto the bit-lines. Writing a value into the SRAM cell is done by forcing one of the bit lines (BIT/BITN) high while keeping the other low. To write a '1' into the SRAM cell, the word line (WL) is Asserted, bit line BIT is made high and bit line BITN is made low. To write a '0' into the SRAM, bit line BIT is made low and BITN is made high. Before reading from the SRAM cell both bit lines (BIT, BITN) are pre-charged high and SRAM cell is selected. When WL selects the SRAM cell to be read, depending on the data in the SRAM cell, one of the bit lines is pulled down. If BIT is pulled down the stored data is '0'. If BITN is pulled down the stored data is '1'. *Sense amplifiers* [12] are used to sense which line is being pulled down and perform the read operation of the stored data. READ and READ_BAR indicate the data stored and its complement during the read operation.

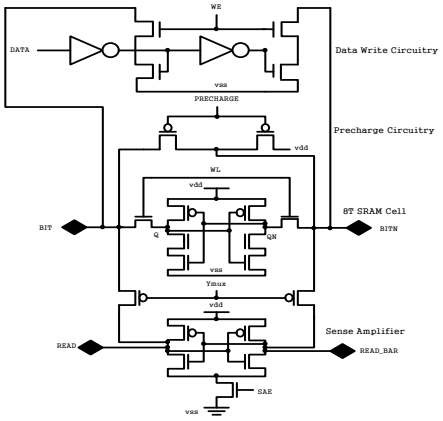

Fig. 3: SRAM Memory System for Writing and Reading Single Bit Data

The single bit memory system comprising of SRAM cell, precharge, data write, column select and sense amplifier is designed and simulated. The complete schematic of data write and read for single cell memory system is shown in Fig. 3. This schematic shows all the different peripherals circuits combined with the static RAM cell, to form a complete working SRAM write and read system. The input signals are write enable (WE) that allows writing of data (DATA) to the SRAM cell, sense (SAE) that allows reading of data from the SRAM cell, word line (WL) that decides to/from which address data will be written or read from and the signal data is the one bit data either 1 or 0 that is to be stored into or read from the SRAM cell. The two output signals are READ corresponding to the data signal and READ_BAR is the inverse of data.

II.8 WORDS X 8 BITS SRAM MEMORY SYSTEM FOR LOW LEAKAGE POWER OPERATION

1. Block Diagram

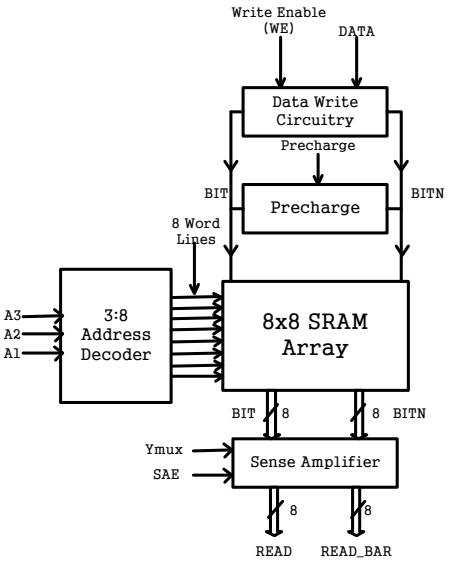

Fig. 4: Block Diagram of 8words x 8bits 8T SRAM Memory System

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Combining the circuits viz, 64 bit 8T SRAM cells, address decoder the precharge circuitry, data write circuitry, and sense amplifiers, 8x8 SRAM array is designed in 90nm technology. The complete setup for data write and read for memory array system is shown in Fig 4. This block diagram shows all the different peripheral circuits combined with the static RAM cells, to form a complete working SRAM 8 x 8 array for write and read operation. Fig. 4 shows the block diagram of SRAM memory with all input signals; precharge, write enable, sense amplifier enable, 8 word lines and 8 input data bits. The 8x8 array for SRAM system is implemented using 64, 8T cells. These are divided into 8 columns of 8 bits each.

2. *Peripheral Circuits*

a) Address decoding:

The proposed SRAM system has storage capacity of 8words of 8bit each. To address these words in a unique manner, 3:8 row decoders are used. Lyon-Schediwy decoder [6] which uses lesser number of transistors than the regular AND/NAND decoder is used for address generation. Since Lyon-Schediwy decoder is a faster decoder, and uses lesser number of transistors, the power dissipation is greatly reduced. It has 3 input lines and 8 output lines. This decoder can accept addresses ranging from 000 to 111. According to the address input the address decoder activates one of the rows by asserting one of the word lines and all the other word address lines remain low. The logical effort of a decoder can be reduced by observing that only one of the outputs will be high so the PMOS transistors can be shared among many outputs. A NOR gates pulls low efficiently through parallel transistor, but has a poor logical effort because the output is pulled high through wide series transistors.

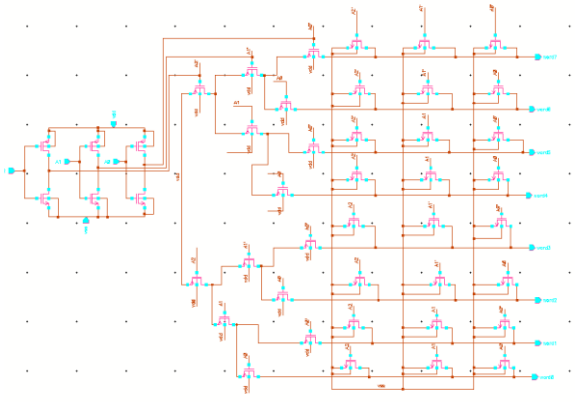

Fig. 5: Lyon-Schediwy 3:8 Row Decoder

The Lyon-Schediwy decoder, as shown in fig. 5, can be viewed as 2^n n-input NOR gates sharing PMOS pull-ups. The 8 words are selected by this 3:8 decoder. The address bits $A_3A_2A_1$ determine the word to be selected for data write or read operation. Only one of the eight address lines is activated in any given time. The 8 selection lines WL_0 to WL_7 are connected to 8 rows of the 8x8 memory array.

b) Precharging:

One pre charging circuit is connected for every column to pre charge the complementary bit-lines, BIT and BITN, to precharged '1' state during inactive state of memory as shown in fig. 3. The signal PRECHARGE is used for this purpose. The precharge circuit is isolated from the bit-lines during the memory write and read operation.

c) Data Write Operation:

Each of the 8 columns of the memory array has one data write circuit as shown in fig. 3. The data write circuit consists of two inverters and an AND gate implemented by pass-transistors. The data write circuitry writes data and its complement onto the bit-lines when activated by write-enable (WE) signal. The data and its complement are written onto the individual nodes Q and QN of the selected word through the access transistors of the SRAM cell.

d) Data Read Operation:

The data written into the SRAM cell is retained as long as the power is present. When the memory is idle i.e. when the memory words are not accessed, the feedback provided by the transistors M7 and M8 help in retaining the memory status. The gates of transistors M7 and M8 are connected to nodes QN and Q respectively as shown in fig. 2. During read operation the sense amplifier enable (SAE) signal is applied to the sense amplifier as shown in fig. 3. This activates the sense amplifier for read operation only for

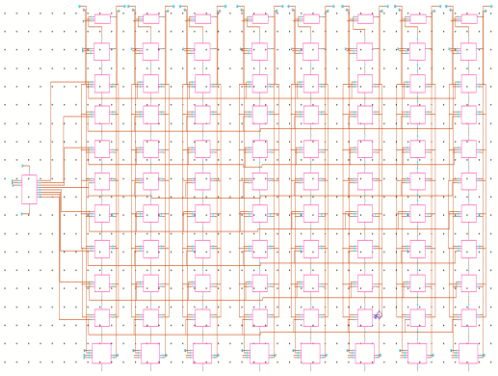

Fig. 6: Top Level Schematic 8 x 8 SRAM System

Short sense duration. At the same time the column is isolated from the bit-lines by using signal Ymux.

This causes one of the bit-lines BIT/BITN to discharge from the precharged value. This creates a differential voltage on the bit-lines which is sensed by the sense amplifier and amplified to the full extent. The data and its complement are reflected on the output lines READ and READ_BAR. The fig. 6 shows the top level schematic of 8 x 8 SRAM system using 8T SRAMs and all above peripherals.

III. SIMULATION AND RESULTS

The simulation results for Power Minimized 8T SRAM array are presented in this section. All simulations were performed with Cadence Virtuoso tool in 90nm GPDK

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process. The designs were simulated across the process corners to make sure that they can withstand the process variations. Finally the entire design as a whole was simulated. Simulations were carried out for the operating temperatures of -50°C to 125°C for 90nm with a power supply voltage of 1.1V. To measure static power dissipation during write operation, WL=1 and one of bit lines BIT is made '1' & other bit line BITN is made '0', to write '1'. BIT=0, BITN=1 to write'0'. When compared to the single bit conventional 6T SRAM cell, it is observed that for the 8T SRAM cell Static Power Dissipation during active mode has reduced considerably by about 16X times. The Static Power Dissipation during idle/standby i.e., WL=0 and SRAM cell bit lines BIT=1 and BITN=1, it is observed that for the 8T SRAM cell Static Power Dissipation during idle mode has reduced considerably by about 16X times when compared to the single 6T SRAM cell. When compared to the total power dissipation of single 6T SRAM cell, it is observed that the single 8T SRAM cell total power reduced by about 3X times. A comparison of the Access Time, Static and Total Power Dissipation in the 8T SRAM cell with 6T SRAM cell are presented in Table. I. Access Time during write and read is calculated for single bit read/write memory system for both 6T SRAM & 8T SRAM. The total power dissipation is also measured. The results are given in Table. II. For 8 x 8 SRAM Array System, the Total Power Dissipation, when compared to 8 x 8 6T SRAM array system, it is observed that the total power dissipation of 8T SRAM 8 x 8 array system has reduced considerably by about 1.28X. The Access Time for both write and read operations is lower as compared to 6T SRAM cell with better data retention. Post-layout simulation of 8T SRAM 8 x 8 array is done. A comparison of the Access Time and Total Power Dissipation in 8T SRAM 8 x 8 arrays with 8 x 8 6T SRAM array systems are presented in Table. III with Post layout 8T SRAM 8 x 8 array results. The wave forms of the 64 bit write data retention and read modes for 8T SRAM 8 x 8 array system are shown in fig.7 and fig. 8. Fig. 9 shows simulation results for 8T SRAM 8 x 8 memory system showing single column reading of data 01010101.A single bit 8T SRAM memory layout is drawn and shown in Fig. 10. The complete memory system layout for 8 x 8 SRAM array is shown in Fig. 11.

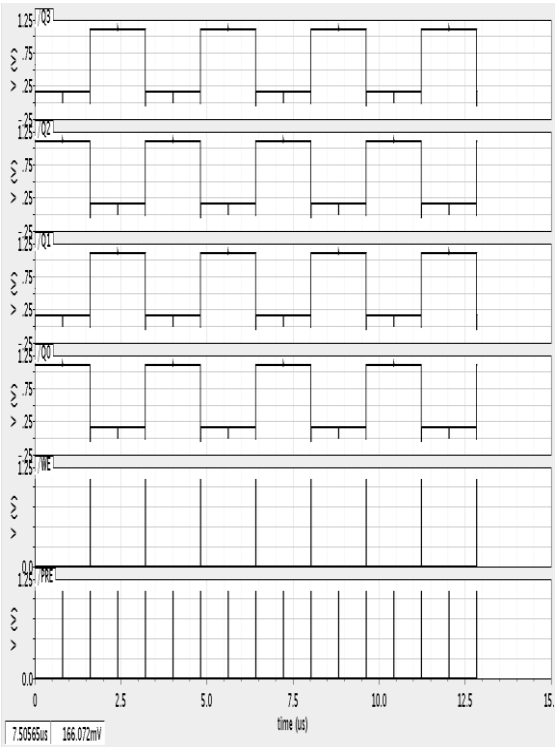
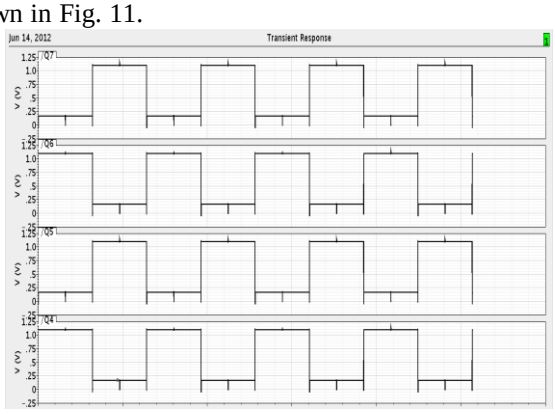
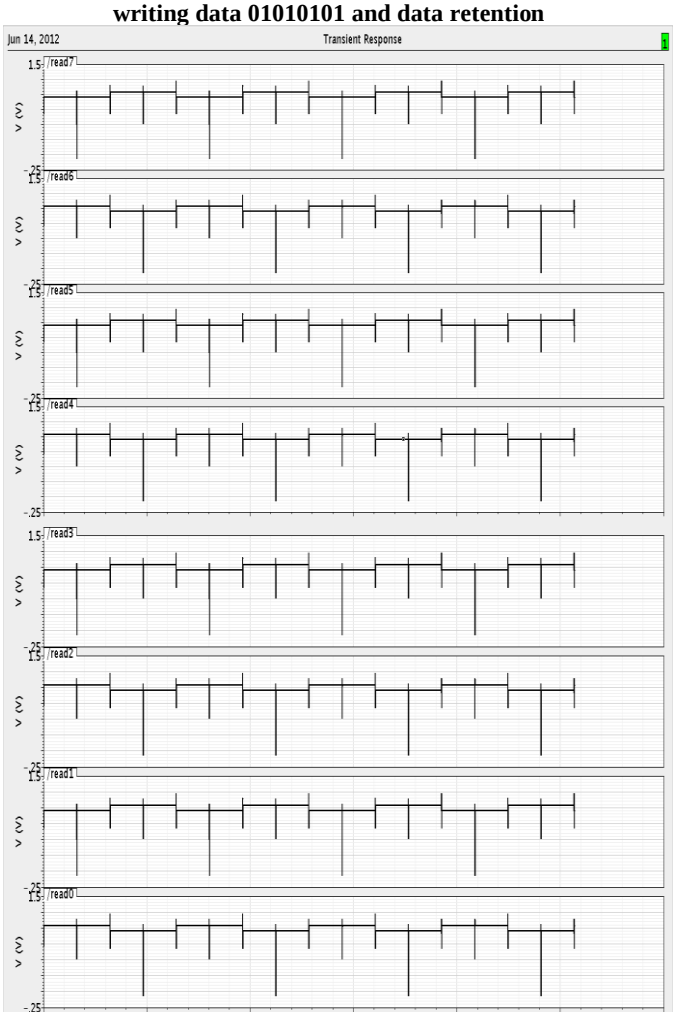


Fig. 7: Simulation results for 8 x 8 SRAM memory system for writing data 01010101 and data retention





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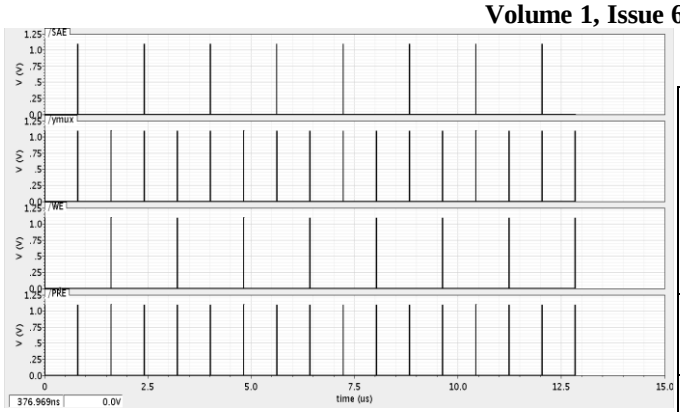

Fig. 8: Simulation results for 8 x8 SRAM memory systems for reading data 01010101

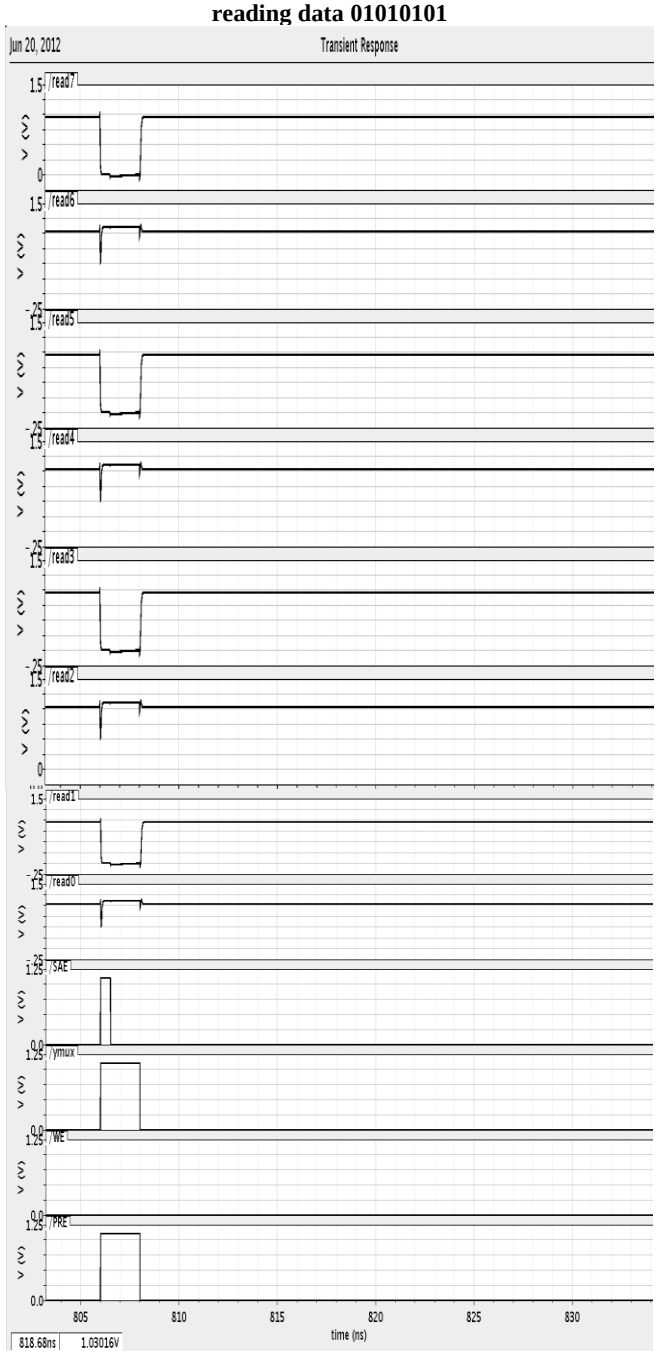

Fig. 9: Simulation results for 8T SRAM 8 x 8 memory system showing single column reading of data 01010101

Table I: Static, Total Power dissipation, and Access Time for Single SRAM cell (Vdd=1.1V)

Single SRAM cell	Static Power		Total Power Dissipation (nW)	Access Time (psec)
	For WL=1, BIT=1 & BITN=0 (nW)	For WL=0, BIT=1 & BITN=1 (nW)		
Conventional 6T SRAM cell	67.542	67.601	115.5	38.901
8T SRAM cell	4.168	4.175	34.07	47.623

Table II: Access Time and Total Power Dissipation for Single Bit SRAM System (Vdd=1.1V)

Single Bit SRAM system	Access Time (psec)		Total power dissipation (nW)
	During write operation	During read operation	During Stop Time 0 to 3us
Conventional 6T SRAM system	199.68	80.989	282.7
8T SRAM system	161.97	81.344	197.7

Table III: Access Time and Total Power dissipation for 8 x8 SRAM array systems (Vdd=1.1V)

8 x 8 SRAM array system	Access Time (psec)		Total power dissipation (mW)
	During write operation	During read operation	During Stop Time 0 to 12.84us
Conventional 6T SRAM 8 x 8 array	913.164	98.0403	3.105
Pre Layout 8T SRAM 8 x 8 array	270.078	95.3036	2.416
Post Layout 8T SRAM 8 x 8 array	301.85	113.766	2.397

The layout was drawn for the design keeping in mind the usage of the block in other designs like ASIC or FPGA. The layout used up to 3 metal layers. So when this memory is used in any ASIC designs metal layers up to metal3 are required. Layout of 8T SRAM cell was made using the *cadence virtuoso layout* tool. As major concern of the project is the power hence the layout is not optimized at its best. Then the *DRC* check was done using *Cadence Assura tool* and no DRC error were found. Also the LVS and RCX check were done with no error. Having successfully made layout of single bit 8T SRAM, layout for 8 x 8 memory system of size 8words x 8bits including all the memory cells and peripherals circuits is made using *Cadence Assura tool*. The layout for 8

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x 8 SRAM array is also successfully drawn and verified for DRC, LVS and RCX Check. Pre layout and Post layout Access Time, Read Time and Total Power dissipation are measured and tabulated in Table III.

IV. LAYOUT

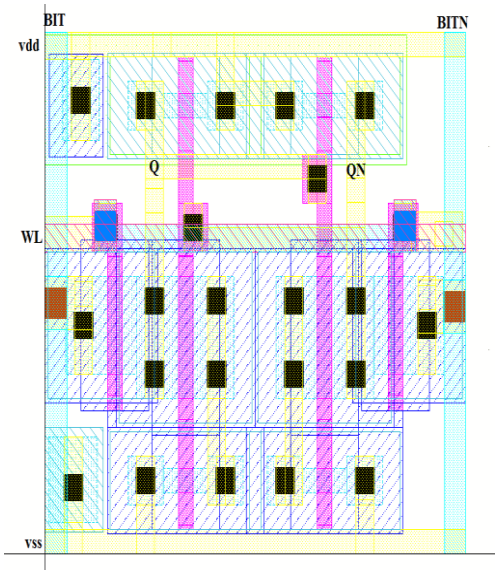

Fig. 10: Layout of single bit 8T SRAM cell

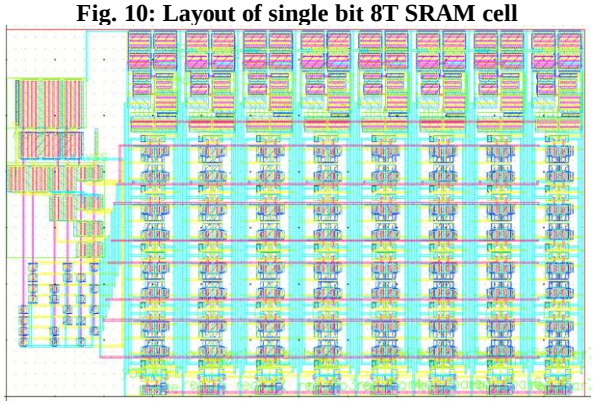

Fig. 11: Layout of 8words x 8bits 8T SRAM Array

V. CONCLUSION

The design and implementation of the SRAM memory proved to be a challenging and valuable learning experience. It gave us the opportunity to learn Cadence Virtuoso tools used in full custom IC design, and also gained deeper understanding of the challenges of deep submicron VLSI design. The static RAM is very widely used in CMOS systems. The 8T cell consists of a cross coupled inverter with two additional NMOS sleep transistor to hold state and two access transistor for differential read and writes. This cell uses internal feedback to reduce dynamic power dissipation as well as the static power dissipation and has excellent stability. The Total Power consumption is also significantly lower as compared to 6T SRAM system along with leakage power reduction during standby mode of operation. The 64 bit 8T SRAM system has lower Access Time compared to 6T SRAM memory system. Hence the low power operation is achieved without sacrificing performance of memory with respect to write and read access time.

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Dr. SY Kulkarni received his B.E degree from BVB College of Engineering and Technology, Hubli and his postgraduate degree in M.Tech as well as doctorate in Electronics & Communications from the reputed, Indian Institute of Technology, Mumbai in the field of VLSI Design. He has a wide range of experience in both the industry and academia. Dr.Kulkarni served at the BVB College of Engineering & Technology, Hubli in various capacities for 15 years. He is currently Principal of Dr. M.S.Ramaiah Institute of Technology, Bangalore. He worked as a Modeling Engineer and Project leader at the GEC Plessy Semi-conductors, Plymoth, UK and as a General Manager at the SASKEN Communication Technologies Ltd., Bangalore. He has also been a visiting faculty for a few universities abroad and has visited the UK and the USA on several assignments. He is a consultant to several semi-conductor companies in Bangalore. He has several technical papers published in national and international journals and is also a recipient of a number of awards. Some of them are : Hon. Membership of the prestigious International Society for Hybrid Microelectronics (ISHM, USA and the International Interconnect Material and Packaging Society (IMAPS, USA), the JAYCEE award "Outstanding Young Indian" and the ISTE Bharatiya Vidya Bhavan National Award for the Best Engineering College Principal for the year 2009 from the Indian Society for Technical Education, New Delhi.