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Implementation and Application of Radar Signal Simulator Based on FPGA

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Abstract*—Radar signal simulator is a device which is used in Ships to monitor the moving or stationary targets on the Plan Position Indicator (PPI). To monitor the targets Radar Signal Simulator requires four kinds of signals. These signals are Sync Pulse, Bearing Pulse, Video Pulse, and Heading Marker Pulse. In this we have implemented the design on FPGA ML-401 board and used EDK & ISE of Xilinx. On ISE we have implemented logic and call our IP on EDK which is taking UART Input from computer to simulate the target .It can capture eight moving target. It is using Graphical User Interface based on Visual Basics to take data.

***Keywords*- EDK, FPGA, IP CORE, ISE, UART, VB.**

I. INTRODUCTION

Radar signal simulator is a device which is used in Ships to monitor the moving or stationary targets on the Plan Position Indicator (PPI).

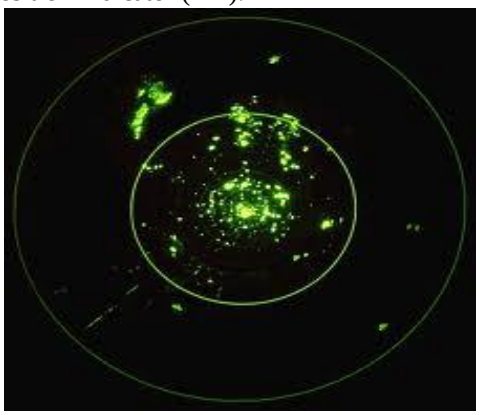

Fig-1 Plan Position Indicator (PPI)

Plan Position Indicator (PPI) as shown in Fig-1, is circular display in which our system always placed at the center where as target is placed at any point located on PPI the range is associated with radius of that dot from the center of PPI. PPI is having requirement of four signals basically Sync Pulse, Bearing Pulse, Video Pulse and Heading Marker Pulse . First of all Sync Pulse is coming. The function of Sync Pulse to generate the beam on the PPI. After that Bearing Pulse is required to rotate the beam appearing on the PPI. Video Pulse has an important role because targets which is appearing on the PPI is depending on the video Pulse if video Pulse is not coming then Targets will not be appeared . To meet the requirements of testing of Radar Signal Simulators, this simulator is generating Video, Heading, Sync, and Bearing Pulses.

Bearing: In ***marine*** navigation, a bearing is the direction one object is from another object, usually, the direction of an object from one's own vessel. In aircraft navigation, a *bearing* is the actual (corrected) compass direction of the forward course of the aircraft. In land navigation, a *bearing* is the angle between a line connecting two points and a north-south line, or *meridian*. Bearings can be measured in two systems, Mills and Degrees.

Ship heading marker: A mark on a direction compass which indicates the position of the ship's head, such as a lubber's line, or an electronic radial sweep line on a PPI (plan position indicator).

Video pulses: Its value is responsible to show the length & breathe of the TARGET on PPI. TARGET Intensity depends on width of video pulses.

Sync Pulse: Beam on the PPI is appeared through the Sync Pulse. Sync Pulse is the first input pulse in the RSS System.

II. BLOCK DIAGRAM

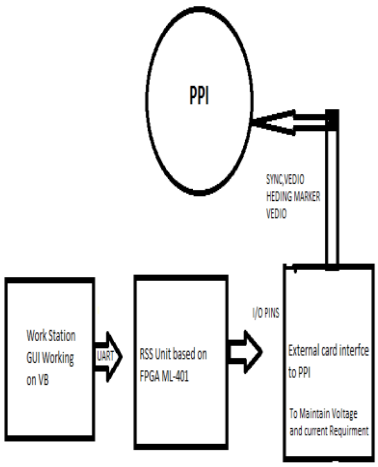

Fig-2 Block Diagram of PPI

Software Section:

FPAGA is taking data from UART of computer using Graphical User Interface which is written on visual basic to send data using COM-1 of work station .this data is used to calculate different fichus target on radar system simulator

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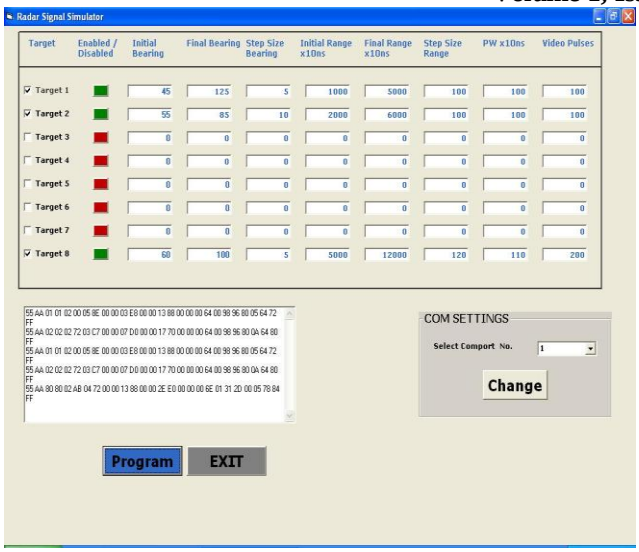

Fig-3 Simulator Interface

The Simulator Interface as shown in FIG- 3 comprises of many inputs and signal output on COM port of computer which is further driven by UART to FPGA BOARD at a standard baud rate of 4800. The packet sent by software is of twenty-eight bits which contain start of packet, end of packet, check sum, number of target, enable/disable of Targets, initial Bearing, final Bearing, step size of Bearing and Range, Pulse width and video pulses. The data send by first button enable and disable the target to be displayed on PPI. Initial Bearing is the angle from which the target is visible on the PPI and final is last point up to which, it displays. Same in the case of initial range and final ranges, it displays the target starting and end range. Its step size means by what steps the target is changing same in case of step size bearing. The pulse width and video pulses combine to give total display area covered by a single target on PPI.

FPGA Section:

It is receiving input from workstation and generating four outputs based on inputs from GUI. By using EDK we have initialize UART lite to a baud rate of 4800 with parity non and stop bit one .Program for generating signals is written on ISE which is called on EDK as IP. The IP is written on Verilog HDL which divides board clock frequency of 100 MHz to 1KHZ by using Counter. A register named **CtrlReg** is used to take data from UART. This register is taking all data for all the eight targets.

Imports peripherals are done by wizard on EDK in which 15 Registers are taken. These registers are further used for control storage and application in generation of signal.

ISE Part:

Module RSS_Top (clk_in, clk 2KHz, clk 1KHz, Out Video Pulse, HeadMark, CtrlReg, TargetReg, Target Status Reg, Init Bearing Reg, Final Bearing Reg, Init Range Reg, Final Range Reg, Pulse Width Reg, Video Pulses Reg, Bearing Offset Reg, Range Offset Reg);

The major criticality is target speed and bearing display on PPI. The bearing pulse is of 2 kHz so that in total 4096 number of pulses generated to display whole circle on PPI .Sync pulse is of 1 kHz and it is coming before all other pulses. The gate pulse which is 23ms width is coming after every 512 bearing pulses. The video is of 10ms-2us width which is coming after every gate pulses. Heading marker is coming after every 4096 pulses to flush all old information present on PPI. Depending on above concept we are using four things for every target 1) Initialization code 2) Moving target code 3) Target pulses 4) IBL_Pulses. At TOP Level every output is combined to generate specific four outputs for eight targets .Counting and timing synchronization is done to get target moving on PPI. The result of simulated value are shown on ISE SIM (FIG-4)

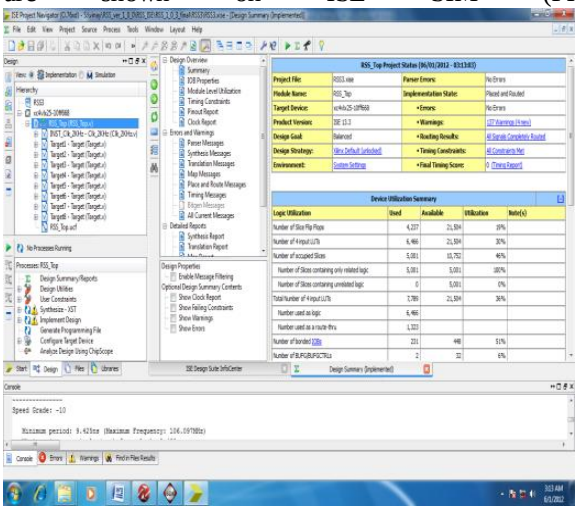

Fig-4 Result of Simulated value on ISE SIM

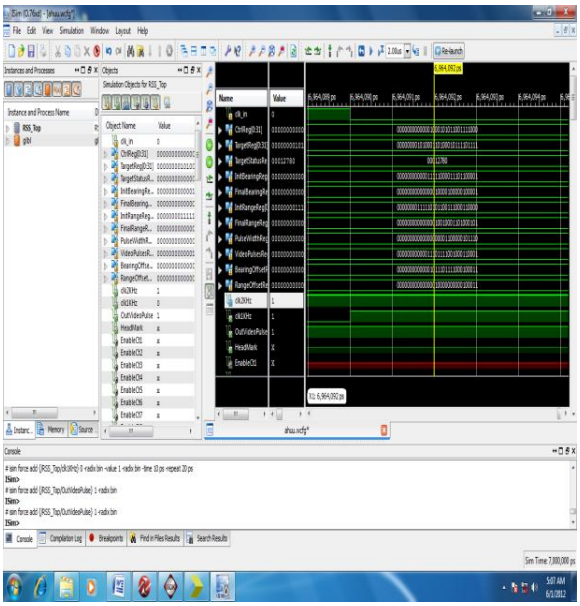

Fig-5 IP of EDK

The imported RSS_Version1 is using 15 registers ,one UART lite ,LEds, General purpose I/Os which is

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connected on PLB bus of FPGA.The imported peripheral is shown in (figure)

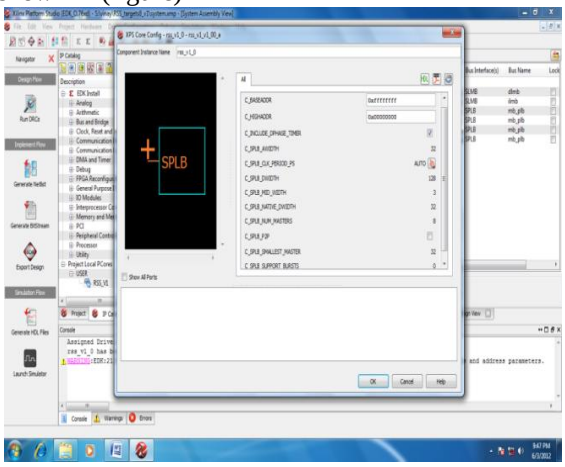

Fig-6 IP specifications

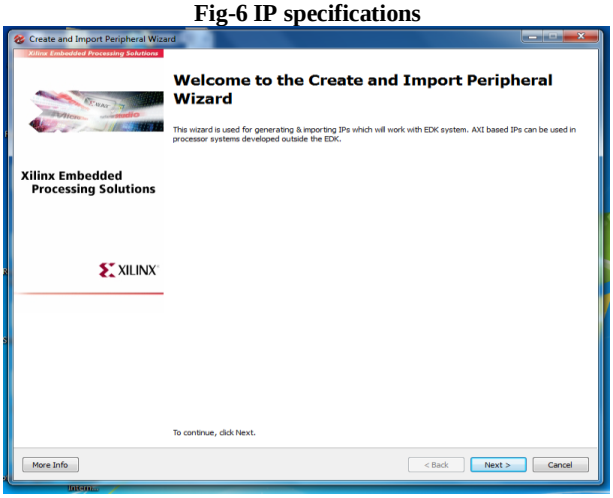

Fig-7 Peripheral wizard import and creation

EDK Part: On EDK we import peripherals of ISE by using create and import peripheral wizard and add this IP named RSS_Version1.0 after adding address is generated. C program is used for writing logics for different Targets. EDK is giving values in control register which is further transfer to generate video of different width to show brightness of Target.

Analog Part: The output of FPGA is of TTL level so its voltage conversion is must and it is done by using diode, OPA-633, CD-40106.The CD-40106 is NOT gate IC It maintains the voltage level to 5v.The Diode stops back current to FPGA and safe GPIOs of it. The OPA-633 is basically used to increase the current driving capability of output.

III.CONCLUSION

In this project RADAR signal Simulator is described first, EDK and ISE is explained to a extent and some part of software design in VB and its implementation on FPGA for further use. In analog part current protection circuit is explained to safe FPGA GPIO Pins.

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