ISSN: 2277-3754
International Journal of Engineering and Innovative Technology (IJEIT)
Volume 1, Issue 4, April 2012

A Simplified SVPWM Algorithm for Multi-Level Inverter fed DTC of Induction Motor Drive

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Abstract*— In this paper a Generalized Space Vector PWM algorithm is proposed for a multi-level inverter. From the sampled reference phase voltages this algorithm generates the inverter leg switching times and centres the middle vector switching times, in a sampled interval. On compared with convention Space Vector topology, the proposed algorithm does not required any sector identification, as a result it reduces the computational time. The present topology is applied to two-level, three-level and five-level inverters and the corresponding results are presented.

***Index Terms*—Space vector PWM, DTC, Multi-Level Inverter, Induction Motor.**

I. INTRODUCTION

As per the industry needs with different applications the adjustable speed drives are becoming popular. The invention of field oriented control (FOC) algorithm has been made a renaissance in the high-performance variable speed drive applications. The FOC algorithm gives the decoupling control of torque and flux of an induction motor drive and control the induction motor similar to a separately excited dc motor [1]. But, the complexity involved in the FOC algorithm is more due to reference frame transformations. To reduce the complexity involved, a new control strategy called as direct torque control (DTC) has been proposed in [2]. A detailed comparison is brought between FOC and DTC in [3] and concluded that DTC gives fast torque response when compared with the FOC. Though, FOC and DTC give fast transient and decoupled control, these operate the inverter at variable switching frequency due to hysteresis controllers. Moreover, the steady state ripples in torque, flux and currents are high in DTC. To reduce the steady state ripples, discrete space vector modulation (DSVM) algorithm has been proposed in [4]. Though, DSVM algorithm reduces the torque ripple up to some extent, it gives variable switching frequency operation of the inverter.

Now a day's many researchers have focused their interest on pulse width modulation (PWM) algorithms to reduce the harmonic distortion and to obtain the constant switching frequency operation of the inverters. A detailed survey on various PWM algorithms is carried out in [5] and concluded that space vector pulse width modulation (SVPWM) algorithm gives good performance. The generation of switching pulses in SVPWM algorithm is given in [6]. Though the SVPWM algorithm gives good performance, the complexity involved is more due to angle and sector calculations. To reduce the complexity involved in SVPWM algorithm, carrier based SVPWM algorithm is developed in [7] by adding the offset voltage to the reference phase voltages. Hence, to reduce the ripples and to obtain the constant switching frequency operation of the inverter, SVPWM algorithm is used for DTC in the literature [8]-[9].The two-level inverter fed DTC drives are suitable for low power applications only. In order to meet the medium and high power applications, nowadays multilevel inverters are becoming popular. A diode clamped three level inverter fed induction motor drive is presented in [10]. A detailed survey on various types of multilevel inverters is given in [11]. But, as the number of levels increases, the complexity involved in the PWM algorithms also increases. To reduce the complexity involved in the SVPWM algorithm, a simplified SVPWM algorithm is presented for three-level inverter in [12].

To reduce the complexity, a novel voltage modulation algorithm is presented in [13] by using the concept of effective time. By extending the same concept, various PWM algorithms have been generated for two-level inverters in [14]. The concept of the PWM algorithms which is presented in [13]-[14] is extended for multilevel inverters in [15].This paper presents a simple generalized scalar PWM algorithm for 2, 3 and 5-level inverters. The proposed algorithm has been developed by using the concept of imaginary switching times, which are proportional to the instantaneous sampled phase voltages only. Moreover, the proposed algorithm does not require the calculation of angle and sector information and hence reduces the complexity involved in the PWM algorithm.

II. SIMPLIFIED SVPWM ALGORITHM FOR TWO-LEVEL INVERTER

The proposed approach is based on the instantaneous values of the reference voltages of a, b and c phases only and the actual switching times for each inverter leg are deduced directly. This method does not depend on the magnitude of the reference voltage space vector and its relative angle with respect to the reference axis. The transformation from two-phase voltages to three-phase voltages can be obtained from the stationary frame reference voltages as given in (1)

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International Journal of Engineering and Innovative Technology (IJEIT)
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$$\begin{bmatrix} V_{an} \\ V_{bn} \\ V_{cn} \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ -1/2 & -\sqrt{3}/2 \\ -1/2 & +\sqrt{3}/2 \end{bmatrix} \begin{bmatrix} V_q \\ V_d \end{bmatrix} \quad (1)$$

If the reference voltage vector lies in the first sector as shown in Fig 1, then the actual switching times can be deduced as

$$T_1 = \frac{3V_{ref}}{2V_{dc}} \frac{Sin(60^o - \alpha)}{Sin60^o} * T_s = \frac{\sqrt{3}}{V_{dc}} \left(\frac{\sqrt{3}}{2} V_{ref} \cos\alpha - \frac{1}{2} V_{ref} \sin\alpha \right) * T_s \quad (2)$$

$$T_2 = \frac{3V_{ref}}{2V_{dc}} \frac{Sin\alpha}{Sin60^o} * T_s = \frac{\sqrt{3}}{V_{dc}} \left(V_{ref} \cos\alpha \right) * T_s \quad (3)$$

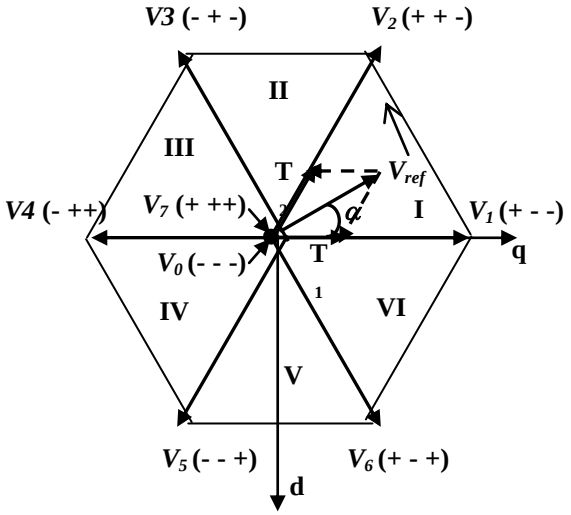

Fig. 1 Voltage space vectors produced by an inverter

But from Fig 1 it can be observed that $V_q = V_{ref} \cos\alpha$ and $V_d = -V_{ref} \sin\alpha$. Hence, the active vector times can be simplified as

$$T_1 = \frac{\sqrt{3}}{V_{dc}} \left(\frac{\sqrt{3}}{2} V_q + \frac{1}{2} V_d \right) * T_s = \frac{T_s}{V_{dc}} \left(V_q + \left(\frac{1}{2} V_q + \frac{\sqrt{3}}{2} V_d \right) \right) * T_s \quad (4)$$

$$= \frac{T_s}{V_{dc}} V_{an} - \frac{T_s}{V_{dc}} V_{bn} \equiv T_{an} - T_{bn}$$

and

$$T_2 = \frac{\sqrt{3}}{V_{dc}} \left(-V_d \right) * T_s = \frac{T_s}{V_{dc}} \left(-\sqrt{3} * V_d \right) = \frac{T_s}{V_{dc}} \left[\left(\frac{-1}{2} V_q - \frac{\sqrt{3}}{2} V_d \right) - \left(\frac{-1}{2} V_q + \frac{\sqrt{3}}{2} V_d \right) \right] \quad (5)$$

$$= \frac{T_s}{V_{dc}} V_{bn} - \frac{T_s}{V_{dc}} V_{cn} \equiv T_{bn} - T_{cn}$$

From (4) – (5), the imaginary switching time periods proportional to the instantaneous values of the reference phase voltages are defined as

$$T_{an} \equiv \left(\frac{T_s}{V_{dc}} \right) V_{an}$$

$$T_{bn} \equiv \left(\frac{T_s}{V_{dc}} \right) V_{bn} \quad (6)$$

$$T_{cn} \equiv \left(\frac{T_s}{V_{dc}} \right) V_{cn}$$

Hence, from (4) – (5), the active vector switching times T_1 and T_2, if the reference voltage vector falls in sector-1 may be expressed as

$$T_1 = T_{an} - T_{bn}\ ; \qquad T_2 = T_{bn} - T_{cn} \quad (7)$$

Thus, the active voltage vector switching times can be represented by the time difference between the imaginary switching time periods. In the SVPWM algorithm, when the reference voltage vector falls in the first sector, the imaginary switching time which is proportional to the a-phase (T_{an}) has a maximum value, the imaginary switching time which is proportional to the c-phase (T_{cn}) has a minimum value and the imaginary switching time which is proportional to the b-phase (T_{bn}) is neither minimum nor maximum switching time. Thus, in general to calculate the active vector switching times, the maximum and minimum values of imaginary switching times are calculated in every sampling time as given in (8) – (9).

$$T_{\max} = Max(T_{an}, T_{bn}, T_{cn}) \quad (8)$$

$$T_{\min} = Min(T_{an}, T_{bn}, T_{cn}) \quad (9)$$

The effective time T_{eff} can be defined as the time difference between $T_{\max}$ and $T_{\min}$ and can be given as in (10).

$$T_{eff} = T_{\max} - T_{\min} \quad (10)$$

The effective time means the duration in which the effective voltage is supplied to the machine terminals. In the actual switching instants, there is one degree of freedom that the effective time can be located anywhere within one sampling interval. To generate actual switching pattern which preserves the effective time, the zero sequence time is subjoined to the phase voltage time. In order to locate the effective time in centre of the sampling interval, the zero sequence voltage has to be symmetrically distributed at the beginning and end of one sampling period. Therefore, the actual switching times for each inverter leg can be simply obtained by the time shifting operation as below.

$$T_{ga} = T_{as} + T_{offset}$$

$$T_{gb} = T_{bs} + T_{offset} \quad (11)$$

$$T_{gc} = T_{cs} + T_{offset}$$

To distribute zero voltage symmetrically during one sampling period, the offset time T_{offset} is achieved using a

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simple sorting algorithm. the zero voltage vector time duration can be calculated as given in (12).

$$T_{zero} = T_s - T_{eff} \quad (12)$$

And, $T_{\min} + T_{offset} \Rightarrow T_{zero}/2$ (13)

Therefore, $T_{offset} = T_{zero}/2 - T_{\min}$ (14)

In order to generate symmetrical switching pulse pattern within two sampling intervals, when the switching sequence is 'ON' sequence, the actual switching time will be replaced by the subtraction value with the sampling time as fallows.

$$T_{ga,gb,gc} = T_s - T_{ga,gb,gc} \quad (15)$$

III. Proposed Generalized PWM Algorithm for n-Level Inverter

In previous section, a simplified algorithm for SVPWM technique has been proposed. For a 2-level inverter only one offset time is sufficient to evaluate the switching instants. Because, in a two-level SVPWM algorithm, in a sampling time interval, the imaginary switching time which has lowest magnitude ($T_{\min}$) crosses the triangular carrier first, and causes the first transition in the inverter switching state. While the imaginary switching time, which has the maximum magnitude ($T_{\max}$), crosses the carrier last and causes the last switching transition in the inverter switching states. Thus the switching periods of the active vectors can be determined from the $T_{\max}$ and $T_{\min}$ in a two-level inverter scheme. But, the sinusoidal PWM algorithm for multilevel inverters, involves comparing the modulating signals with a number of symmetrical level-shifted triangular carrier waves for PWM generation. It has been shown that for an n-level inverter, n-1 level-shifted triangular carrier waves are required for comparison with the sinusoidal references. Because of the level-shifted multicarriers, the first crossing (termed the first-cross) of the reference phase voltage cannot always be the min-phase. Similarly, the last crossing (termed the third-cross) of the reference phase voltage cannot always be the max-phase. Thus the offset time, which is given in the previous section, is not sufficient to centre the middle inverter switching vectors, in a multilevel PWM scheme during a sampling period Ts.

In this section, a simple technique to determine the offset voltage or offset time (to be added to the reference phase voltages for PWM generation for the entire modulation range) is presented, based only on the instantaneous imaginary switching times which are proportional to sampled amplitudes of the reference phase voltages. The idea behind the proposed scheme is to determine the sampled reference phase, from the three sampled reference phases, which crosses the triangular first (first-cross) and the reference phase which crosses the triangular carrier last (third-cross). Once the first-cross phase and third-cross phase are identified, the principles of offset calculation of (14), for the two-level inverter, can easily be adapted for the multilevel SVPWM generation scheme. The proposed generalized PWM algorithm presents a simple way to determine the time instants at which the three reference phases cross the triangular carriers. These time instants are sorted to find the offset voltage to be added to the reference phase voltages for SVPWM generation for multilevel inverters for the entire linear modulation range, so that the middle inverter switching vectors are centred (during a sampling interval), as in the case of the conventional two-level SVPWM scheme.

For a n-level inverter, in the proposed generalized PWM algorithm, the instantaneous imaginary switching times, which are proportional to the instantaneous sampled reference phase voltages are calculated as follows:

$$T_{as} = V_{an} \times \frac{T_s}{V_{dc}/(n-1)} \quad (16)$$

$$T_{bs} = V_{bn} \times \frac{T_s}{V_{dc}/(n-1)} \quad (17)$$

$$T_{cs} = V_{cn} \times \frac{T_s}{V_{dc}/(n-1)} \quad (18)$$

Where *n* represents number of levels.

The time equivalent of a common mode voltage is termed as $T_{offset1}$ which can be defined as

$$T_{offset1} = -(T_{\max} + T_{\min})/2 \quad (19)$$

Where $T_{\max}$ and $T_{\min}$ are the maximum and minimum of T_{as}, T_{bs} and T_{cs}. Then time equivalents of the modified phase voltage magnitudes can be defined as

$$T_{as}^{*} = T_{as} + T_{offset1} \quad (20)$$

$$T_{bs}^{*} = T_{bs} + T_{offset1} \quad (21)$$

$$T_{cs}^{*} = T_{cs} + T_{offset1} \quad (22)$$

As already discussed for a n-level inverter the modulating waves are compared with n-1 level shifted triangular carriers. The triangular carriers and the modulating waves, for an n-level PWM scheme are shown in Fig.2a, for n is odd, and in Fig. 2b, for n is even. The (n-1) triangular carriers are compared with reference phase voltages as shown in Figs. 3a and 3b.

A carrier index, I, is defined to designate the carrier regions in which the reference phase voltages lie during the sampling interval under consideration. The indexing of I is as shown in Fig. 2a when n is odd. The carrier index I for the top carrier is 1, and it increases in steps of 1 towards the bottom carriers. The carrier index I for the lowest carrier is equal to (n–1). During a sampling interval, the carrier indices, I_a, I_b and I_c (which can be from 1 to n-1), for a, b and c phases, respectively, are determined depending on the carrier region in which the respective phase voltage lies. Then the time durations, $T_{a-cross}$, $T_{b-cross}$ and $T_{c-cross}$ when n is odd, can be determined for a n-level inverter as:

$$T_{a\_cross} = T_{as}^{*} + ((I_a - (n-1)/2) * T_s \quad (23)$$

ISSN: 2277-3754
International Journal of Engineering and Innovative Technology (IJEIT)
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$$T_{b\_cross} = I_{bs}^{*} + ((I_b - (n-1)/2) * T_s \quad (24)$$

$$T_{c\_cross} = T_{cs}^{*} + ((I_c - (n-1)/2) * T_s \quad (25)$$

When n is even, the triangular carriers and the reference phase voltages, are as shown in Fig.2b. In this case, the reference phase voltages are centered on the middle triangular carrier. Then the time durations, $T_{a-cross}$, $T_{b-cross}$ and $T_{c-cross}$ when n is even, can be determined for a n-level inverter as:

$$T_{a\_cross} = (T_s/2) + T_{as}^{*} + ((I_a - (n/2)) * T_s) \quad (26)$$

$$T_{b\_cross} = (T_s/2) + T_{bs}^{*} + ((I_b - (n/2)) * T_s) \quad (27)$$

$$T_{c\_cross} = (T_s/2) + T_{cs}^{*} + ((I_c - (n/2)) * T_s) \quad (28)$$

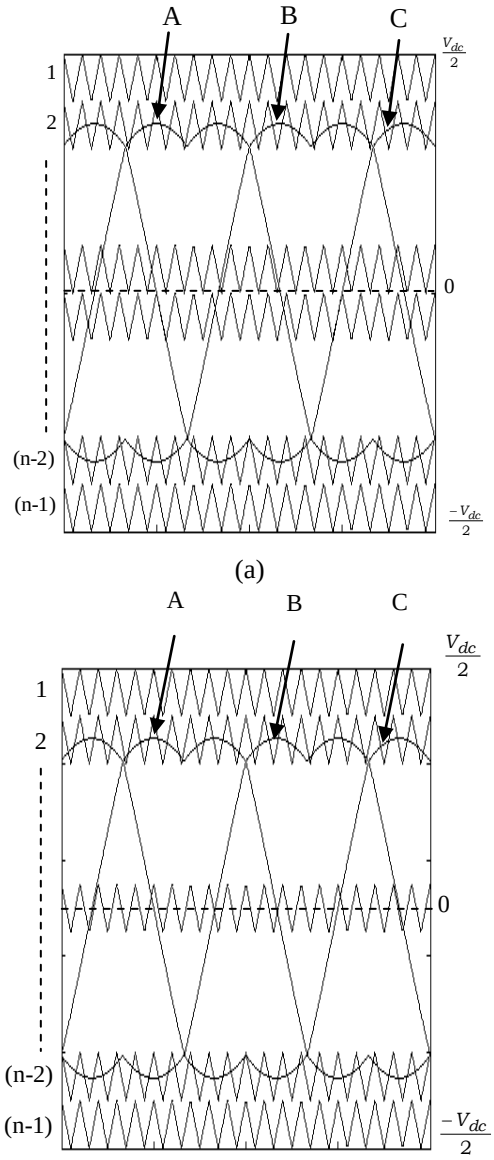

Fig.2 triangular carrier and reference signals (a) n-level PWM scheme where n is even (b) n-level PWM scheme where n is even

In the proposed generalized PWM algorithm, the $T_{a-cross}$, $T_{b-cross}$ and $T_{c-cross}$ are used to centre the middle switching vectors as in the case of two-level inverters in each sampling time interval. The time-duration, at which the reference phases cross the triangular carriers for the first time, second time and third time are defined as T_{first_cross}, T_{second_cross} and T_{third_cross} respectively, in a sampling time interval T_s. these can be calculated from (29).

$$\begin{aligned} T_{first\_cross} &= \min(T_{x\_cross}) \\ T_{second\_cross} &= mid(T_{x\_cross}) \\ T_{third\_cross} &= \max(T_{x\_cross}); \quad x = a,b,c \end{aligned} \quad (29)$$

During one sampling interval Ts, the time durations T_{first_cross}, T_{second_cross} and T_{third_cross} directly decides the switching times for different inverter voltage vectors, forming a triangular sector. A time offset, $T_{offset2}$ is added to T_{first_cross}, T_{second_cross} and T_{third_cross} to centre the middle vector. The offset time, $T_{offset2}$ is determined as follows: The time duration for the middle inverter switching vectors, T_{middle}, is given as

$$T_{middle} = T_{third\_cross} - T_{first\_cross} \quad (30)$$

The time duration for start and end vector is

$$T_0 = T_s - T_{middle}. \quad (31)$$

The time duration for start vector is given by

$$T_0/2 = T_{first\_cross} + T_{offset2} \quad (32)$$

Therefore, $T_{offset2} = T_0/2 - T_{first\_cross}$ (33)

By adding the time, $T_{offset2}$ to T_{first_cross}, T_{second_cross} and T_{third_cross} gives the inverter leg switching times T_{ga}, T_{gb} and T_{gc} for phases a, b and c, respectively as (34)-(36).

$$T_{ga} = T_{a\_cross} + T_{offset2} \quad (34)$$

$$T_{gb} = T_{b\_cross} + T_{offset2} \quad (35)$$

$$T_{gc} = T_{c\_cross} + T_{offset2} \quad (36)$$

IV. RESULTS

Matlab-Simulink based simulation studies have been carried out to validate the proposed simplified SVPWM algorithm based 2-, 3-, and 5- level inverter fed DTC-IM drive. The simulation parameters and specifications of induction motor used are R_s = 1.57Ω, R_r = 1.21Ω, L_s = L_r = 0.17H, L_m = 0.165H and J = 0.089Kg.m^2 are considered. The steady state simulation results for conventional DTC, 2-, 3-, and 5-, level inverter fed DTC-IM drive are shown from Fig. 3 to Fig. 15.The average switching frequency of the inverter is taken as 3 kHz. For the simulation, the reference flux is taken as 1wb and starting torque is limited to 40 N-m. From the simulation results it can be observed that as the number of levels increases the harmonic distortion will be decreased. Also, it can be concluded that the proposed PWM algorithm is efficient with reduced complexity.

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International Journal of Engineering and Innovative Technology (IJEIT)
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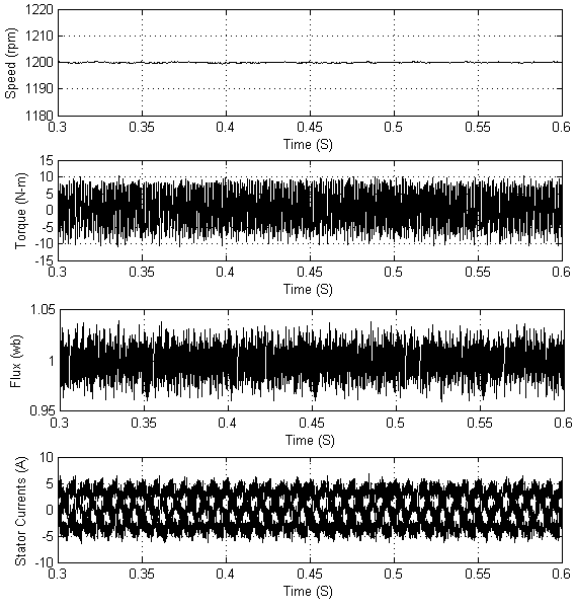

Fig.3.Simulation results of Conventional DTC: steady-state plots of speed, torque, currents and flux at 1200 rpm

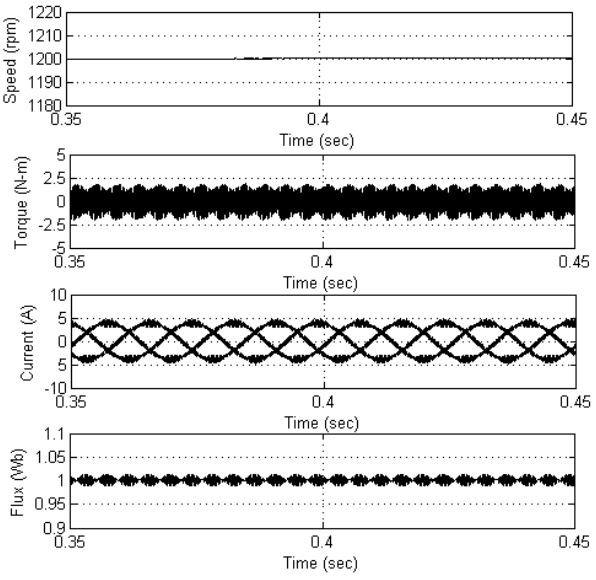

Fig.4 Simulation results of 2-level SVPWM based DTC: steady-state plots of speed, torque, currents and flux at 1200 rpm

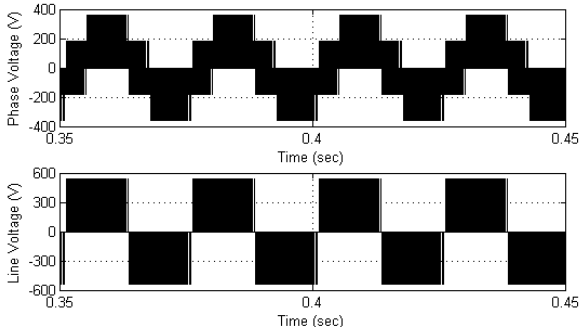

Fig. 5 Simulation results of 2-level SVPWM based DTC: steady state plots of phase and line voltages

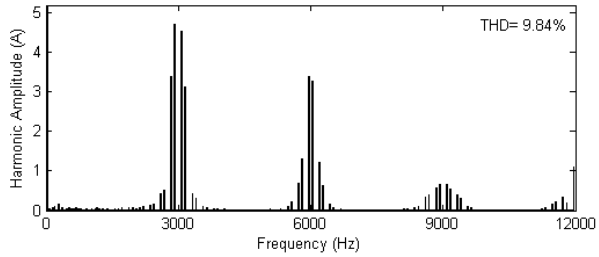

Fig. 6 Harmonic Spectrum of line current for 2-level SVPWM based DTC along with THD

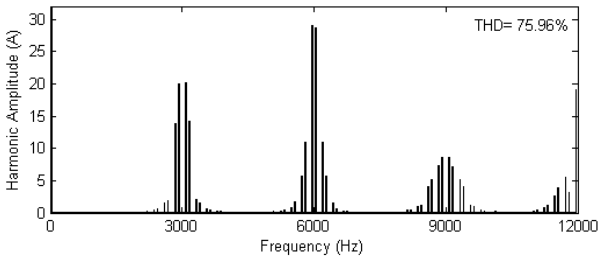

Fig. 7 Harmonic Spectrum of line voltage for 2-level SVPWM based DTC along with THD

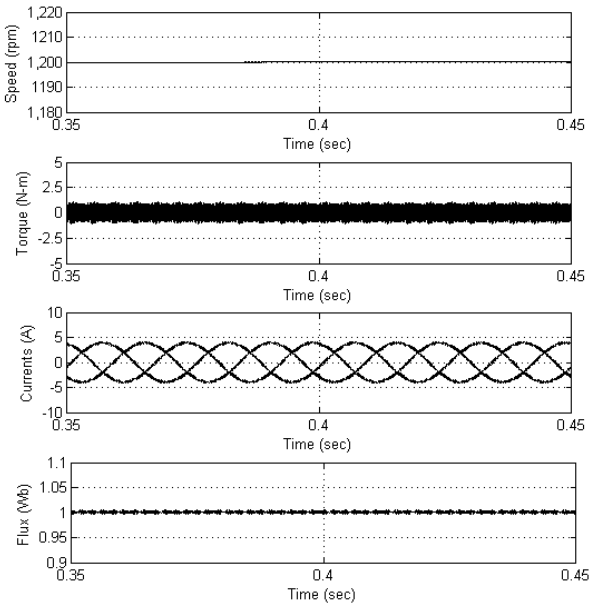

Fig.8 Simulation results of 3-level SVPWM based DTC: steady-state plots of speed, torque, currents and flux at 1200 rpm

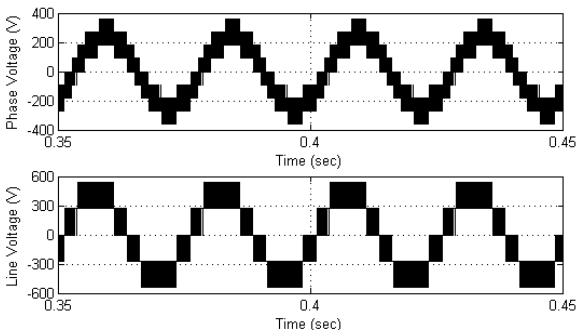

Fig.9 Simulation results of 3-level SVPWM based DTC: steady state plots of phase and line voltages

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International Journal of Engineering and Innovative Technology (IJEIT)
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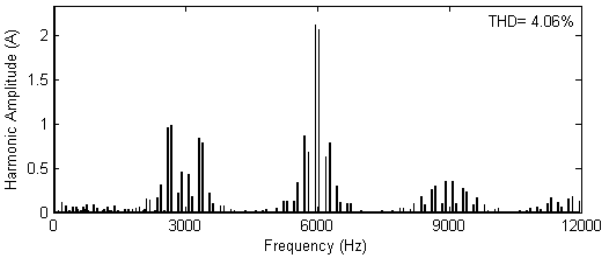

Fig.10 Harmonic Spectrum of line current for 3-level SVPWM based DTC along with THD.

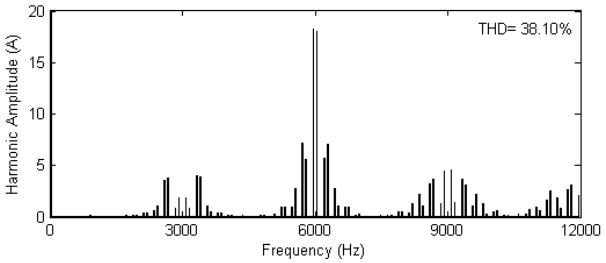

Fig. 11 Harmonic Spectrum of line voltage for 3-level SVPWM based DTC along with THD.

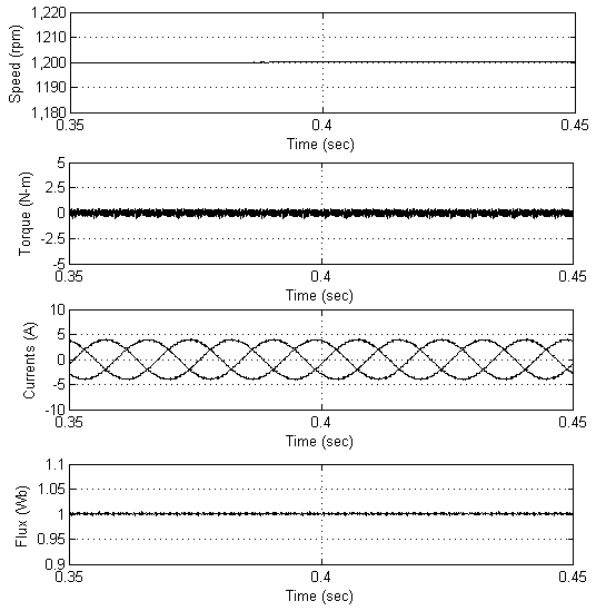

Fig. 12 Simulation results of 5-level SVPWM based DTC: steady-state plots of speed, torque, currents and flux at 1200 rpm

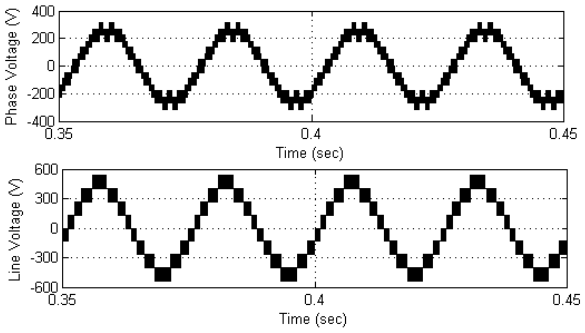

Fig. 13 Simulation results of 5-level SVPWM based DTC: steady state plots of phase and line voltages

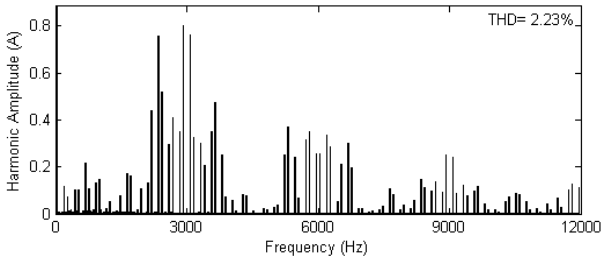

Fig. 14 Harmonic Spectrum of line current for 5-level SVPWM based DTC along with THD

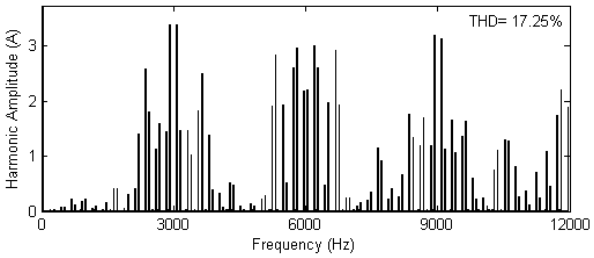

Fig. 15 Harmonic Spectrum of line voltage for 5-level SVPWM based DTC along with THD

V. CONCLUSION

Though the classical DTC gives fast dynamic performance, it gives large steady state ripples and variable switching frequency operation of the inverter. To reduce the ripples and to achieve constant switching frequency operation of the inverter, a simple and generalized PWM algorithm for an n-level inverter fed DTC-IM drive is presented in this paper. To validate the proposed PWM algorithm, numerical simulation studies have been carried out and results are presented. From the simulation results, it can be observed that the multilevel inverter fed DTC drive gives less harmonic distortion and ripples.

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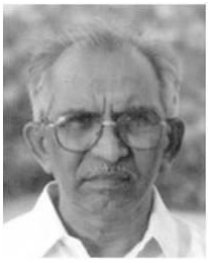

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