ISSN: 2277-3754
International Journal of Engineering and Innovative Technology (IJEIT)
Volume 1, Issue 2, February 2012

A Low Power Estimation Technique for Logic Gates in VLSI

B. Mohan kumar Naik, Dr.Ananth
Research Scholar, Singhania University

Abstract-- The low Power estimation is an important aspect in digital VLSI circuit design. The estimation includes a power dissipation of a circuit. The number of inputs and their combinations. The power estimations are specific to a particular component of power. the process of optimization of circuits for low power, user should know the effects of design techniques on each component . There are different power dissipation methods for reduction in power component. Therefore it is necessary to provide the information about the effect on each of these components .Hence in this paper estimating the power like short circuit and the total power has taken.

I. INTRODUCTION

Estimating the short circuit dissipation has been coupled with the dynamic dissipation and report the switching energy. The short circuit current flow has its characteristics and to be studied. The short circuit models are proposed and studied .The correct model taken into account of capacitance load effect, the input rise and fall times. The overall current flow can be determined by the rise and fall time. The short Circuit current flows can be taken by load capacitance during the charging or discharging of the node capacitance. So with this larger output load means a decrease in short circuit current. This method is to accurately and efficiently estimate the different power components for digital VLSI technologies. The circuit level power estimation can accurately and efficiently estimate various power components and the total power and provide information to a designer. With the modification and significant advances made in logic simulation, timing analysis and delay areas through the use of the bounded delay model and also be extended to include leakage power.

II. POWER DISSIPATION IN CMOS CIRCUITS

There are three main sources of power dissipation in CMOS circuits:

- Dynamic power
- Short circuit power
- Leakage power

Dynamic power dissipation: The dynamic power dissipation is the charging or discharging of the nodal capacitances during a high to low or low to high transition at the output node. The nodal capacitance of the internal capacitance of the gate, the interconnect wire capacitance of the fan out and the gate capacitances of the corresponding fan out gates.

Short circuit power dissipation: The short circuit current is the period during in which the transistors switching action and are potentially on state, which provides a conducting path from the gate. Where single transition is enough to reach the final value. This is known as the logic transition and with that the logic power component can be determined.

Leakage power dissipation: The leakage power can be neglected when compared to the dynamic power consumption. But for nano CMOS technologies, leakage power becomes a important component of the total power. The leakage power can be credited to reverse bias the PN junctions and the sub threshold leakage current.

III. SHORT CIRCUIT POWER ESTIMATION

When transistors are switching in the"ON" state, providing a conducting path from the supply to ground. Which intern flows a short circuit current? This is equal to shorting the supply and ground terminals .For a very short duration within the rise or fall time of the input this will happens .This power dissipation also depends on the how much current will flow from the supply voltage to charge or discharge the capacitance. Output loading capacitances .The current which remains will be the short circuit current, and output node capacitance will reduce the overall short circuit current. Therefore the short circuit current will be at maximum lower capacitive loads and when the output rise and fall times are much smaller than the input signal rise and fall times. The rising waveform Vi (t) is applied to the input of an inverter with the corresponding output Vo(t) . The short circuit current Isc(t) waveform that peaks at time t2 when the PMOS transistor goes from linear to saturation .

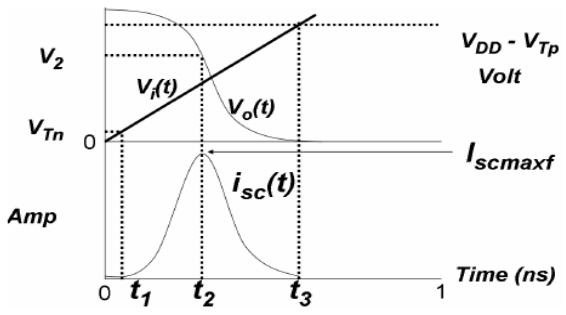

Fig. 1. Short-circuit scenario

From the above figure depict in a case of a rising input of an inverter. During the time period t1 to t2, the NMOS transistor will be in the saturation region and the PMOS transistor will be in the triode region. Therefore the peak short circuit current flows from the PMOS transistor triode region to the saturation region. After estimating the peak current, calculating the area under the short circuit current can be done .There after estimate for the total short circuit flowing during

ISSN: 2277-3754
International Journal of Engineering and Innovative Technology (IJEIT)
Volume 1, Issue 2, February 2012

this period will be taken care The estimation of the peak short circuit is calculated . By using the time period t1 to t2 the current discharging through the NMOS transistor when it is in the saturation region can be modeled by the differential equation:

$$-\frac{C_L}{V_{dd}}\frac{dv_{out}}{dt} = 0.5K_n(v_{in}-n)^2$$

Where vin − n < vout and where CL is the load capacitance, Vdd is the supply voltage,vout is the output voltage, Kn is the Tran conductance of the NMOS transistor, vin is the input voltage and n is the threshold voltage. Upon integration the output voltage with respect to time t can be found as:

$$v_{out} = 1-\frac{V_{dd}K_nt_0}{6C_L}(\frac{t}{t_0}-n)^3$$

$$v_{in}(t) = \frac{t}{t_0}$$

Where t0 is the rise time of the input signal and t ∈ [0, t0]. From the above equations the component of the current through the PMOS transistor can be neglected. Therefore this creates inaccurate estimation of short circuit current as the PMOS current is can not negligible comparing with current flowing through the NMOS transistor. With this over estimating the short circuit current can be happen .With the correction factor scaling can be done with SPICE simulations. The above equation is rewritten as:

$$v_{out} = 1-\frac{1}{6}(\frac{V_{dd}K_nt_0}{C_L})^{\epsilon}(\frac{t}{t_0}-n)^3$$

Where ϱ is the correction factor. The value of ϱ varies with input rise time value t0, CL is output load capacitance and The Tran conductance factor Kp. Then ε can be formulated as:

$$\epsilon = \epsilon_0K_p+\epsilon_1t_0+\epsilon_2C_L+\epsilon_3$$

Technology parameters then can be done from SPICE simulations. To estimate the peak current the output voltage at time t2 from the above equations. Calculate the time t2 by replacing vout = vin −pin, will be the output voltage just at the time PMOS starts go to saturation. From the third order polynomial one real solution for t2. after estimating the output voltage at time t2, using the drain current equations we can estimate the current flowing through the PMOS transistor and then calculate the area under the short circuit current curve to get the total short circuit current flowing during this period .Thus we can then depict the short circuit energy calculated as:

$$E_{scf} = \int_{t_1}^{t_3} V_{dd}I_{sc}(t)\,dt = (t_3-t_1)I_{scfmax}\frac{V_{dd}}{2}$$

Where Vdd is the supply voltage, Isc(t) is the short circuit flowing at time t, and Isc fmax is the peak short circuit current. For gates other than inverters, like NAND/NOR, they are converted into equivalent sized inverters and the short circuit current is estimated. These are approximate reasonable results. This is a reasonable approach as parallel transistors can be modeled as equivalent sized transistors without any loss in accuracy, and series transistors complexity increases due to multiple nodes and different regions of operation the transistors. During the short circuit estimation, the series connected transistors are not considered during the charging or discharging period, this is a parasitic behavior, as studied and can be modeled with sufficient accuracy with equivalent sized transistor. The complex gates are broken down to smaller gates and then modeled as equivalent sized inverter to estimate the short circuit current.

IV. SUMMARY

The estimation techniques are implemented for logic gate level estimation tool. The tool can estimate the different power dissipation components and also estimate the power dissipation while maintaining efficiency .Also capable of separating and estimating the different power dissipation components. The above technique can be used for estimating a short circuit current. There have been other notable works focusing on particular power components. Due to the size of the problem, that there are few works that estimate and separate each component with notable accuracy and efficiency.

REFERENCES

[1] L. Bisdounis, S. Nikolaidis, and O. Loufopavlou, “Propagation Delay and Short-Circuit Power Dissipation Modeling of the CMOS Inverter,” IEEE Trans. Circuits and Systems I: Fundamental Theory and Applications, vol. 45, no. 3, pp. 259–270, Mar. 1998.

[2] S. Bobba and I. N. Hajj, “Maximum Leakage Power Estimation for CMOS Circuits,” in Proc.15th International Conf. on VLSI Design and 7th Asia and South Pacific Design Automation Conf., Jan. 1999, pp. 116–124.

[3] A. Bogiolo, L. Benini, and B. Ricc`o, “Power Estimation of Cell-Based CMOS Circuits,” in Proc. Design Automation Conf., 1996, pp. 433–438.

[4] A. Boliolo, L. Benini, G. de Micheli, and B. Ricco, “Gate-Level Power and Current Simulation of CMOS Integrated Circuits,” IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 5, pp. 473–488, Dec. 1997.

[5] S. Bose and V. D. Agrawal, “Delay Test Quality Evaluation Using Bounded Gate Delays,”Proc. 25th IEEE VLSI Test Symp, May 2007, pp. 23–28.

[6] S. Bose, H. Grimes, and V. D. Agrawal, “Delay Fault Simulation.

[7] H. Grimes, “Reconvergent Fan-out Analysis of Bounded Gate Delay Faults,” Master’s thesis, Auburn University, Aug. 2008. Dept. of ECE.

[8] H. Grimes and V. D. Agrawal, “Analyzing Reconvergent Fanouts in Gate Delay Fault Simulation,” in Proc. 17th IEEE North Atlantic Test Workshop, May 2008, pp. 98–103.

ISSN: 2277-3754
International Journal of Engineering and Innovative Technology (IJEIT)
Volume 1, Issue 2, February 2012

[9] R. X. Gu andM. I. Elmasry, "Power Dissipation Analysis and Optimization of Deep Submicron Circuits," IEEE Journal of Solid-State Circuits, pp. 707–713, May 1996.

[10] S. Hassoun, "Critical Path Analysis Using a Dynamically Bounded Delay Model," in Proc. 37th Design Automation Conf., 2000, pp. 260–265.