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Sampling frequency adaptive algorithm for reducing spectral leakage

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Abstract: ***In this paper, an adaptive sampling frequency algorithm is implemented to overcome spectral leakage associated with FFT, when sampling frequency is not synchronous with actual signal frequency. FFT analysis is carried out with C8051F120, 8 bit microcontroller. With on-chip 12 bit DAC sinusoidal waveform of different frequency is synthesized. Principal wave frequency is set to 50 Hz as the foundational sampling frequency, then the actual signal frequency is obtained with software algorithm, and sampling frequency of ADC is adjusted in real-time to improve accuracy. From the results, it is found that with adaptive sampling frequency the spectral leakage reduces.***

***Index Terms*—** **FFT, spectral leakage.**

I. INTRODUCTION

Fast Fourier transformation (FFT) based on discrete-time sampling is the main method in harmonic detection and analysis. The FFT algorithm, first explained by Cooley and Tukey, reduces the order of complexity of DFT from N^2 to N $\log_2 N$ [1].There are three dangers in using the FFT to compute the DFT. These are aliasing, picket-fence effect and leakage [2]. Aliasing is a condition wherein high frequency components translate to low frequencies if the sampling rate is lower than twice the highest frequency in the signal. The picket-fence effect is caused by frequencies which are not an integer multiple of the fundamental frequency. Spectral leakage arises when the sampling frequency is not synchronous with the actual signal frequency.

Avoiding the picket-fence effect and the spectral leakage requires more effort since these effects are mainly due to the sampling in the frequency domain and the waveform truncation, which come from the nature of the FFT process. To overcome the spectral leakage, adaptive sampling frequency algorithm is implemented. This improves accuracy of spectral analysis and harmonic measurement.

II. STANDARD RADIX-2 DIT-FFT ALGORITHM ANALYSIS

Fig.1, shows data flow diagram for 3 stages, obtained from $\log_2 8$. There are 4 butterfly operations in every stage, so 4 * 3 = 12 butterfly operations are needed to complete 8 point radix-2 DIT FFT. Every butterfly operation needs two data and a twiddle-factor. Data is stored in ram and the twiddle-factor can be calculated or read from ROM. Practice shows that bit-reversion of the input time- domain data is more favorable [3].

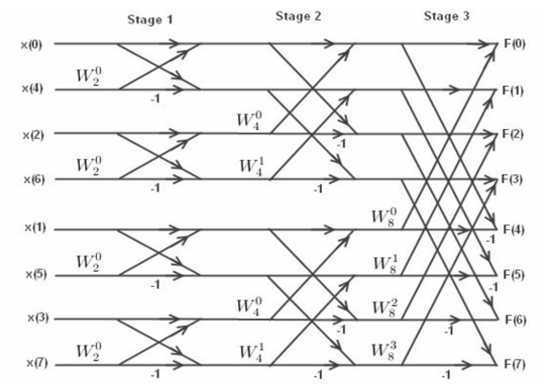

Fig.1.Butterfly diagram for 8 point FFT [4]

A. Selection of sampling rate

Sampling is the first step in representing a continuous time signal in a discrete time or a digital signal. It is necessary to select number of samples to be collected before performing FFT. The data collection time interval must be long enough to satisfy desired FFT frequency resolution for the given sample rate [5].The number of points of FFT (N) is given by

$$N = \frac{f_s}{resolution} \quad \text{Where } f_s \text{ is sample rate}$$

Unlike the audio signal, frequency variation in power line frequency is low. Normally power line frequency variation is from 48.5 Hz to 51.5 Hz. Nominal power line frequency is 50 Hz, so to consider 20th harmonic as the highest harmonic component of interest, the signal frequency is 1000Hz. The sampling frequency of the ADC should be chosen to satisfy Nyquist criteria.

If we need frequency resolution of 10 Hz, then for sampling frequency of 10 KHz, the number of points will be 1000. As N must be integral power of 2, we select 1024 points & for that sampling rate is (1024*10) =10240Hz.

B. Realization of frequency adaptation algorithm

Frequency measurement algorithm is realized with C8051F120 - 8 bit microcontroller. For frequency measurement, timer is used in capture mode. In this mode timer operates as 16 bit counter/timer with capture facility. A high to low transition on the T2EX input pin causes the 16-bit value in the associated timer to be loaded into the capture registers. From this count value real time frequency is measured. This frequency is used to calculate sampling

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frequency of ADC. Flow diagram for frequency adaptive algorithm is shown in fig 2.

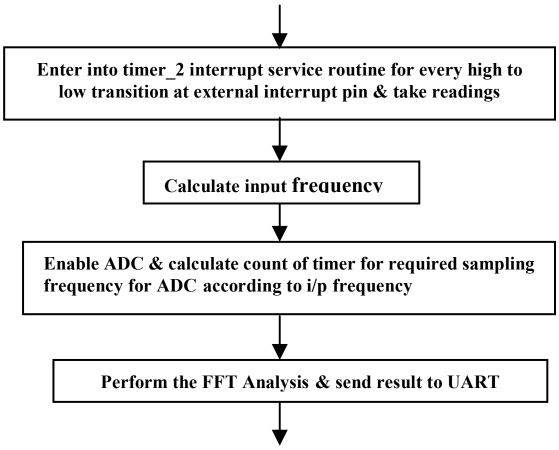

Fig 2: Flow diagram for frequency adaptive algorithm

C. Description of performed FFT

ADC0 collects the data to process and it is stored in the array. The 12-bit ADC data is left-justified and stored as 16-bit data with trailing zeros. After the data has been collected, it is windowed using the selected window. The window calculation function performs a multiplication of each input sample with its corresponding value in the window table. It also changes data that has been stored in single-ended format into differential format. This centers the data about 0x0000 to remove the DC bias. For changing between normal order and bit reversed order, each data point is swapped with another location in the data set determined by reversing the order of the bits in the sample index.

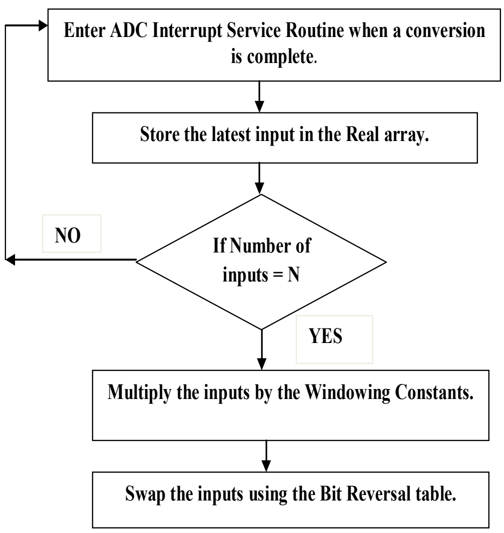

Fig: 3 Flow diagram for FFT analysis

To reduce computation time, sine and cosine values are not calculated in real-time. Instead, they are pre-calculated and stored in code space. During the first stage of the FFT, it is assumed that all imaginary locations are equal to zero.

III. RESULTS OF DIFFERENT SAMPLING FREQUENCY

Here results of FFT analysis with adaptive sampling algorithm and the fixed sampling algorithm are shown. I observed that for fixed sampling, magnitude of fundamental component decrease due to frequency variation. While the adaptive sampling algorithm, can follow the actual frequency and reduce the spectral leakage when the frequency of the signal fluctuates.1024 point FFT is performed with 10 Hz frequency resolution. Different frequencies with variation of ±1 Hz are considered as input frequencies to ADC.

A. Input frequency=50 Hz

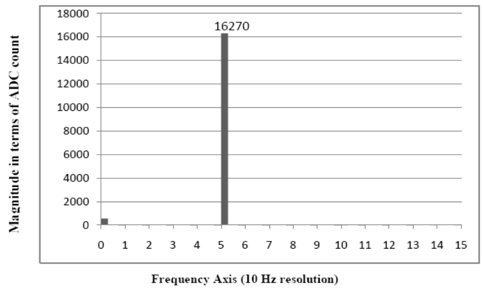

Fig: 4(a) FFT analysis with fixed sampling freqency=10240 Hz.

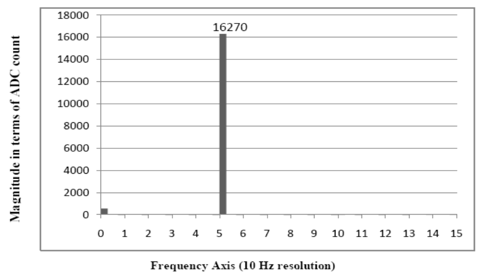

Fig: 4(b) FFT analysis with adaptive sampling freqency.

B. Input frequency=51.02 Hz

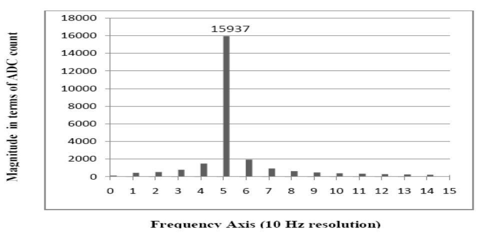

Fig : 5(a) FFT analysis with fixed sampling freqency=10240 Hz.

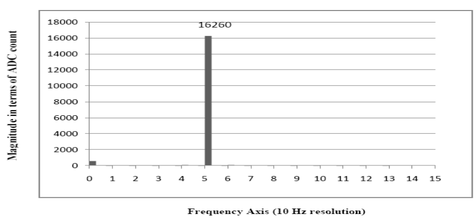

Fig : 5(b) FFT analysis with adaptive sampling freqency.

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C. Input frequency=52.08 Hz

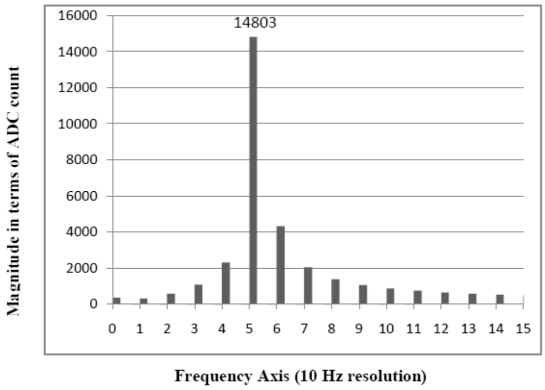

Fig: 6(a) FFT analysis with fixed sampling freqency=10240 Hz

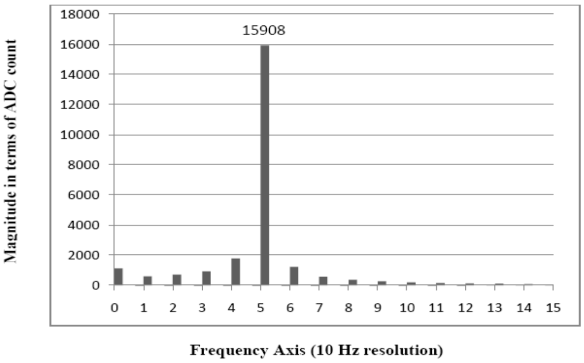

Fig: 6(b) FFT analysis with adaptive sampling freqency.

D. Input frequency=49.02 Hz

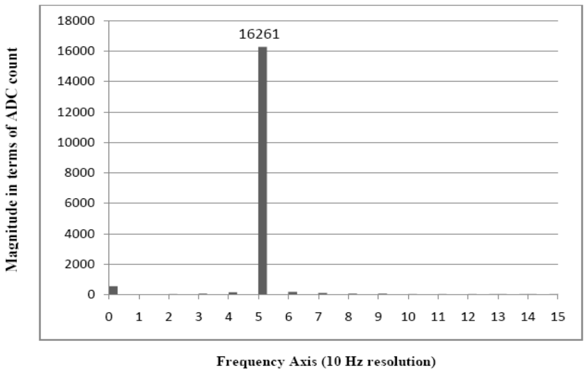

Fig: 7(a) FFT analysis with fixed sampling freqency=10240 Hz

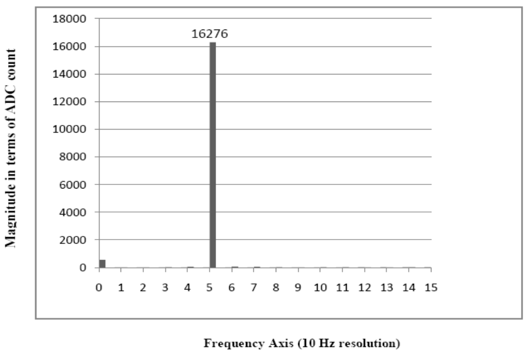

Fig: 7(b) FFT analysis with adaptive sampling freqency.

E. Input frequency =48.08 Hz

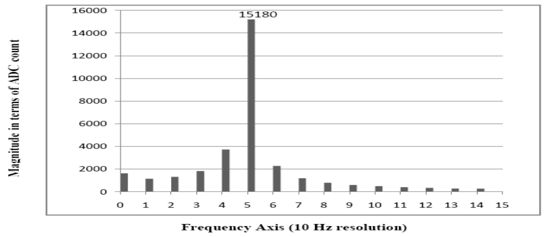

Fig: 8(a) FFT analysis with fixed sampling freqency=10240 Hz

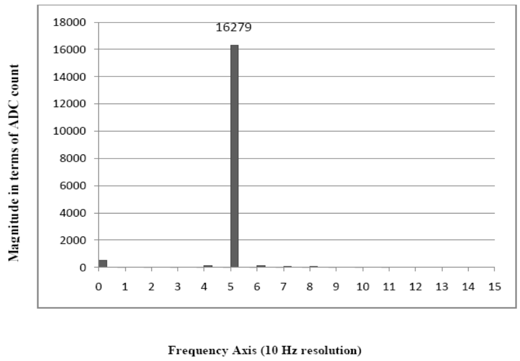

Fig: 8(b) FFT analysis with adaptive sampling freqency.

From the above results it is seen that for fixed sampling, magnitude of fundamental component decrease due to frequency variation. From Fig.6 (a), for input frequency of 52.08Hz, the magnitude of fundamental should be ≈16270 (ADC count), instead the magnitude is reduced to 14803 and it is leaked into neighboring bins. While Fig.6 (b) shows that the adaptive sampling algorithm, can follow the actual frequency and reduce the spectral leakage when the frequency of the signal fluctuates. Similarly we can see that as deviation from fundamental frequency increases, leakage also increases.

IV. CONCLUSION

8 bit microcontroller with CIP-51 core running at 49.76 MHz (30 to 40 MIPS) was found to be capable enough to perform the real time FFT. Adaptive sampling frequency algorithm is developed which reduces FFT leakage in presence of frequency variation.

REFERENCES

[1] Cooley, J., and Tukey, J, “An algorithm for the machine computation of the complex Fourier series,” Math. Computat, pp. 297–301, 1965.

[2] Girgis, A. A. and F. M. Ham. “A qualitative study of pitfalls in the FFT” I. IEEE Transactions on Aerospace and Electronic Systems, vol. AES-16, no. 4, 1980.

[3] Yiyuan Wang, Ping Li, Yiwen Wang, Hui Li, “Low-Power High-Speed Radix-2 DIT FFT Suitable for AAC/DRA Audio Decoding” IEEE conference Computer Network and Multimedia Technology, 2009.

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[4] "An explanation on 8 input butterflies", [online] Available: http://www.alwayslearn.com/DFT%20and%20FFT%20Tutorial/DFTandFFT_FFT_Butterfly_8_Input.html [Accessed: April 15, 2011].

[5] Lyons, R. G. "Understanding Digital Signal Processing", Addison Wesley Longman, Inc., Reading, Massachusetts, 1997.

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Jayana Rana (ISTE Member), graduated from the Sarvajanik College of Engineering and Technology in India (B.E. Instrumentation and Control Engineering) in 2003 and completed Post Graduation from Sardar Vallabhbhai National Institute of Technology in India (M.Tech in Power Electronics and Drives) in 2011.From 2004 to 2010, she was a lecturer in Sarvajanik College of Engineering and Technology and in 2010 she was promoted to Assistant Professor in Instrumentation and Control Department.