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Implementation of Different Current Commutation Technique in Matrix Converter

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Abstract-Matrix converter is emerging to be an alternative topology for power converters, drive by persistent cost reduction of silicon devices and the development of reverse blocking IGBTs. One of the major obstacles towards commercial acceptance of this topology has been the commutation of the bi directional switches. A detailed study has been made here to understand the limitations and possible improvement of the existing current commutation techniques. In this paper, FPGA implementation of a semi-soft four step commutation techniques based on output current direction in matrix converter is presented. The same program can be used for implementing three-step commutation process. A universal and synchronous commutation scheme for all the IGBTs is devised so that commutation can smoothly take place as and when required within the minimum possible time depending on the switching time of the IGBT used. The different aspects of this commutation are verified through MATLB simulink.

***Index* Terms—Matrix Converter, Bi-directional switch, Current commutation.**

I. INTRODUCTION

Power frequency changer is an integral part of ac drive applications. From power quality point of view, it is desirable to use a compact voltage source converter to provide sinusoidal output voltages with varying amplitude and frequency, while drawing sinusoidal input currents with unity power factor from the ac source. Matrix converter is an array of controlled bi-directional switches that connects directly a three-phase source to a three phase load (Fig. 1). This topology, which has progressively developed over the last two decades, offers a nearly all semiconductor solution for AC-to-AC power conversion. Despite being equipped with some of the most desirable features for any power converter, commercial exploitation of this topology has been held back due to some practical limitations.

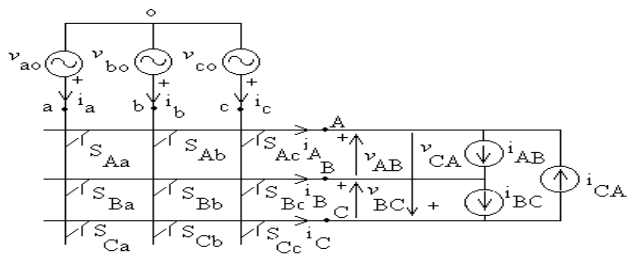

Fig.1.Matrix converter circuit

One of these issues has been the problem of current commutation, which, of late has been the focus of considerable attention and many schemes have been proposed to address this issue [1]-[7].

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(a) Simple and compact power circuit
(b) Generation of load voltage of arbitrary amplitude and frequency
(c) Nearly sinusoidal input and output currents
(d) Control over input power factor irrespective of loads
(e) Bi-directional power flow

II. REALISATION OF BIDIRECTIONAL SWITCH

There are three possible configurations for realizing a bi-directional switch [5]:

- Diode Bridge with a single IGBT as shown in Fig. 2(a)
- A pair of Back to Back IGBTs in common collector mode as shown in Fig.2(b)
- A pair of Back to Back IGBTs in common emitter mode as shown in Fig. 2(c)

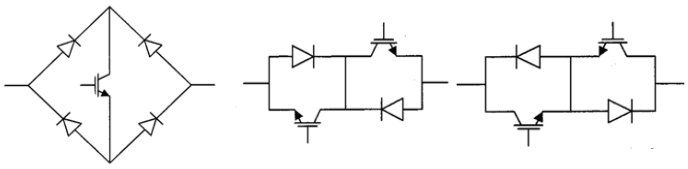

Fig. 2. Realization of bi-directional switch (a) diode bridge with single IGBT, (b) common collector configuration, (c) common emitter configuration

i) Diode Bridge Switch Configuration

A diode bridge arrangement with one switching device providing the current path at all times is shown in Fig.2(a)This configuration of bi-directional switch has the advantage of requiring only one IGBT and one associated gate driver circuit. The disadvantage of this arrangement is that three devices are always conducting at any time. This gives rise to relatively high conduction losses [3].

(ii) Back- to-Back IGBT in common collector configuration

A back-to-back arrangement of two IGBTs with their collector common may be used to implement the bi-directional switch as shown in Fig.2(b). The two diodes are used to provide the reverse-voltage blocking capability. This arrangement was chosen for use in practice for certain advantages. (1) Independent control of the current in both directions. This facility can be used to reduce the switching losses during commutation of the load current. (2) The back-to-back arrangement also has lower conduction losses than a diode bridge switch arrangement as fewer devices are conducting at any given time. (3) In the common-collector configuration, the emitter of each device is connected to either an input or an output line of the converter. With this configuration the number of isolated power supplies required by the gate drivers for the converter is reduced to six [5]

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(iii) Back- to-Back IGBT in common emitter configuration

The IGBTs may be connected in common-emitter configuration as shown in Fig. 2(c). This configuration has similar advantages like (1) Independent control of the current in both directions. This facility can be used to reduce the switching losses during commutation of the load current and (2) The back-to-back arrangement also has lower conduction losses than a diode bridge switch arrangement as fewer devices are conducting at any given time. (3) If the devices in the switch are connected with common emitters then only one isolated power supply is required for gate drive circuits to drive both the switches in a cell although if independent control of each IGBT in a pair is required, there must still be an independent gate drive circuit for each device. Therefore, the number of isolated power supply required for this type of connection is nine for nine switch cells.

III. CURRENT COMMUTATION

The process of turning off a conducting semiconductor and transferring the current to another switch is known as "commutation" [4]. Current commutation is an integral part of a matrix converter realization where load current needs to be transferred in any one of the three input phases depending on the modulation logic through one of the three different bi-directional switch cells connecting a output phase to the input phases as shown in Fig.1. A switch cell is generally constructed using IGBTs and diodes in various configurations for medium power applications [2].

The general rule that has to be adhered to while considering any control strategy for a matrix converter is that each output phase must have only one switch cell connected to an input phase at any time at steady state. This prevents the input from being short-circuited and at the same time provides continuous current through the inductive load at output Whenever there is a requirement of changing the input phase connected to a particular output phase, the current flowing through the output phase needs to be transferred from outgoing input phase to incoming input phase instantaneously without any disruption of the output current considering the load is inductive. Reliable current commutation between switch cells of matrix converters is more difficult to achieve than in conventional VSIs due to the absence of natural freewheeling paths. The commutation needs to be actively controlled all the time with respect to the switching rule stated above and illustrated in Fig.3. To attenuate the high frequency component in the input current L-C filters are used in the input. The output inductances signify that, during switching, the output load is considered as constant current load. [2]

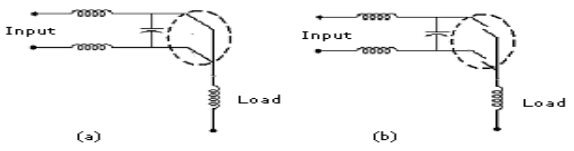

Fig. 3. Unwanted switching: (a) short circuit at input lines (b) open circuit at output lines

These two switching considerations make the task difficult to implement because (1) IGBTs are not identical and their inherent finite switching delays are different,(2) gate drive circuits' response times are different. Therefore, devices cannot be turned on or off at the same instant.

Different schemes are in use for commutation [4]. The schemes follow the switching constraints and also take into account the finite switching times of the semiconductor devices and sensor delays. Some of these rely on the output current direction, while others rely on relative magnitudes of input voltages to activate the commutation stages. However, the disadvantages of relative voltage based commutation method outweighs its advantages as has been pointed out in [6] where the commutation time has been shown to be greater than the methods relying on output current directions. The main disadvantage of output current detection based commutation is that the offset errors make erroneous signals for commutation logic for which output may be open circuited causing over voltage. However, this is of no major concern because of a clamp circuit connected between the input and output terminals [2] can be used to effectively counter this problem. The over voltages can appear from the input side, originated by line voltage perturbations. Also, dangerous over voltages can appear from the output side, caused by an over current fault. When the switches are turned off following an over current fault, the current in the inductive load is suddenly interrupted. The energy stored in the motor inductance has to be discharged without creating dangerous over voltages. A clamp circuit, as shown in Fig.4, is the most common solution to avoid the over voltages coming from the grid and from the motor. This clamp configuration uses 12 fast-recovery diodes to connect the capacitor to the input and output terminals.

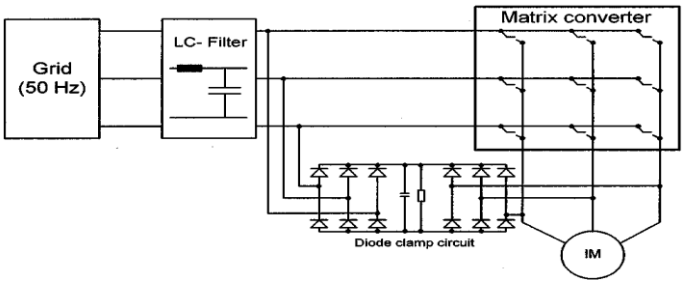

Fig. 4. Matrix converter with clamp circuit

Therefore, the method using output current direction information has been considered here for further improvement in commutation time. The output current direction can be sensed by using either output current sensors or by measuring the voltages across each device in a bi-directional switch cells which was proposed and had been covered in details in [7]. The process allows the current to commutate from one switch to another without causing a line-to-line short circuit or a load to be open circuited. This commutation is known as "semi-soft" commutation since 50% of the switching is by devices that are reverse biased. This implementation is asynchronous. In this method data transfer is not based on predetermined timing pattern and is

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limited by frequent interactions between the sensor circuits during the commutation process. This adds unwanted delays of the sensing devices to the commutation process. The total time taken by the commutation process cannot be estimated quantitatively. A large number of sensing circuitry (one voltage sensor per IGBT device) has to be used to implement the method. The sensors need to interact in between themselves as well as the gate driver during the commutation process. This makes the control scheme complicated and offsets the other advantages of two-step commutation using voltage measurements across the switching devices.

In this paper, a generalized, synchronous switching logic for current commutation based on output current direction [8] is considered for detail study and further improvement. The advantages of this schemes are (1) entire process of commutation is a synchronous one, (2) is not affected by delays from current sensor circuits and (3) commutation time can be conveniently estimated and fixed for any commutation requirement occurring anytime and anywhere in the circuit. This time is also programmable depending on the switching times of the semiconductor devices. The commutation time used here (1.6 μs) for four-step commutation considering a particular type of IGBTs [9]. This is negligible compared to the sampling period of pulse width modulation of 20 KHz (1.6 μs << 50 μs). However, for subintervals of the duty cycles, this commutation time may be significant. But this limit should be adhered to for safe commutation. The commutation sub-intervals are general and hence, are applicable for all switching devices including IGBTs. The commutation process is described in the following section.

IV. GENERALISED SYNCHRONOUS CURRENT DIRECTION BASED COMMUTATION METHOD

The commutation scheme is explained with the help of a two-phase to single phase matrix converter is shown in Fig.5. The two phase to single phase matrix converter is considered to make the analysis simple but rigorous. The two ac voltage sources of same magnitude and phase but with phase differences are the two input supply phases to the matrix converter. Two bi-directional switch cells connect those two phases to the single phase load. The switch cells are composed of two emitter-coupled back to back IGBTs with inverse parallel connected diodes.

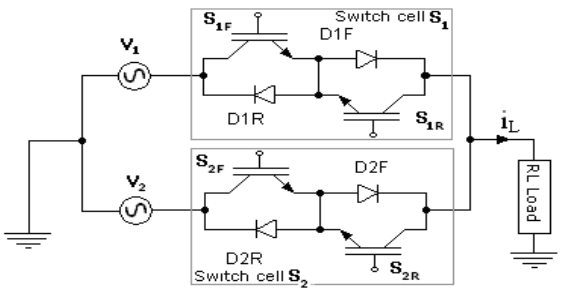

Fig.5. Two phase to single phase matrix converter considered in the scheme.

The modulation pulses for these switches obeys the constrains of switching i.e. at any instant of time either of the switch cells must get switch –on gating pulse when the other receives switch-off gating pulse.

In an active cell, two unidirectional devices are connected in such a way so that current in both the direction can flow. In conducting state, both of the devices in the active cell are gated to allow both directions of current flow. At a particular instant of time, one of the devices is taking the current. The other device in the same cell is reverse biased by the forward biased diode connected across it as shown in Fig.5. This is required because IGBts considered here cannot block reverse voltage. This device can be said to stay at "OFF" condition, although it has the turning-on gate voltage.

A. Four step commutation

We consider the circuit shown in Fig.5. It is assumed that at the instant of time considered, the load current (iL) is in the direction shown and that the upper bi-directional switch S1 is closed i.e. active. When a commutation to S2 is required, the current direction is used to determine which device in the active cell is not conducting. This device (in this case, S1R) is then turned off first. The device that will conduct the current in the incoming switch is then gated (S2F in this example) after a time duration t_{C1}. The load current begins to divert to the incoming device. The outgoing device (S1F) is turned off just after the incoming device S2F (time interval t_{C2}) starts sharing the load current. The load current is completely transferred to the incoming device after certain time depending on the incoming voltage and circuit parameters. The remaining device in the incoming switch (S2R) is turned on after time duration t_{C3} assuming the outgoing device will turn-off completely after this time interval. This will allow current reversals in steady state. This precaution is taken to prevent input short circuit. The process is illustrated by the timing diagram as shown in Fig.6.

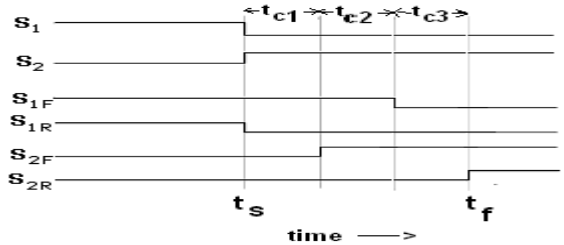

Fig. 6:- Four step current commutation

B. Three step commutation

In the case of a three step commutation method, S2F and S1F has to be turned on and off at the same instant. The corresponding timing diagram is shown in the Fig.7. Since turn off time of an IGBT is greater than the turn on time under all operating conditions [4], both the switching transitions can take place without violating the output open circuit switching constraint and this will further reduce the overall commutation time. There will be a definite problem

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at low current level due to offset in the current sensors for which the output current direction might be erroneously indicated. Then the conducting IGBTs may be switched off causing output voltage spike. For example, if S1R is turned off at first by wrongly sensing the current direction as positive, the excessive voltage will occur across the switches. The snubbers (R-C) across IGBTs can reduce the voltage spike [4]. For a large capacity IGBTs, resistance for the snubber must be set low to reduce heat dissipation and turn-on losses. For frequent change in the voltages across snubber, losses in snubber itself are quite large. So, it is not suitable for high frequency pulse width modulated matrix converter. However, this spike is reduced by a diode bridge clamp circuit commonly connected between output and input terminals as an extra protection circuit which clamps the output voltage level within the input voltage magnitude [2]

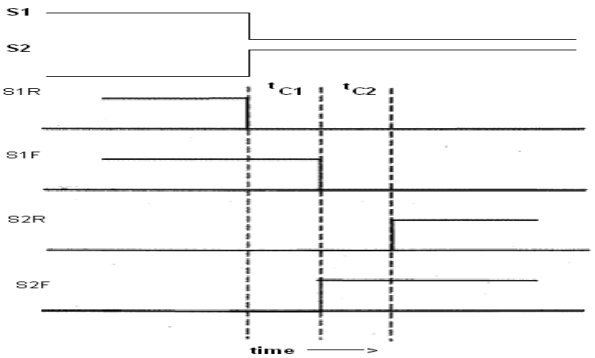

Fig. 7 Three step commutation

C. Single step commutation

In the case of a single-step commutation method, S_{1F}, S_{1R} are turned off by reverse bias gate voltage according to the modulation signal and at the same instant of time, S_{2F} and S_{2R} get the turned-on gate pulses. The corresponding timing diagram is shown in Fig.8. The turn-off gate pulses make the outgoing conducting IGBT S1F to be turned off after the turn-off time and make the non-conducting IGBT S1R turned-off quickly (will take less time than the conducting IGBT because of absence of tailing current effect and no storage charge in the drift region). The turn-on gate pulses for the incoming switch cell S2 make the incoming IGBT S2F turned-on within the turn-on time of the IGBT and make the non-conducting IGBT S2R turned-on. There is a possibility of short circuit current for a very short duration when both the IGBT S1F and S1R are in their turning-off and turning –on phase respectively. But this duration is negligibly small because the other incoming IGBT S2F while begins to share the load current make the diode across the IGBT S2R in forward conducting mode. The forward voltage drop across this diode set reverse voltage across the collector emitter of the IGBT S2R making it OFF. Usually the IGBTs are rated to withstand this small duration short circuit current and the input L-C filter reduces the level of this short circuit current. The single-step commutation has advantage of not sacrificing the modulation pulse width for commutation. There is no requirement of current sensors also [8].

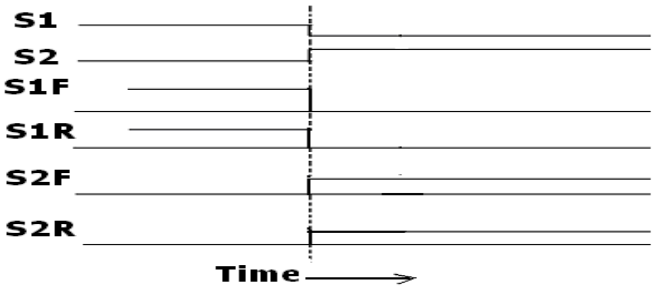

Fig. 8 Single step current commutation

V. REVIEW OF THE IMPLEMENTATION OF CURRENT COMMUTATION LOGIC USING FPGA

The different commutation logic by output current sensing was implemented using FPGA [8]. The implementation scheme is briefly discussed here. A 3x3 matrix converter is considered as shown in Fig.1. There are three blocks of bi-directional switches [S11, S12, S13],[S21, S22, S23] and [S31, S32, S33], that connect three different inputs to the same output. The switching restrictions subject switches in each block to the condition.

$S_{11} + S_{12} + S_{13} = 1$
$S_{21} + S_{22} + S_{23} = 1$
$S_{31} + S_{32} + S_{33} = 1$

Where a single switch cell takes the value 1 when closed and 0 when open.

LC-Filters are used at the input of the matrix converters to reduce the switching frequency harmonics present in the input current [2]. A universal switching logic applicable to each of the IGBTs has been devised for each block connected to a output phase keeping in mind the switching constraints. A schematic of the logic block, which is responsible for correctly sequencing the steps of commutation of a single IGBT switch in a block, is shown in Fig.9.

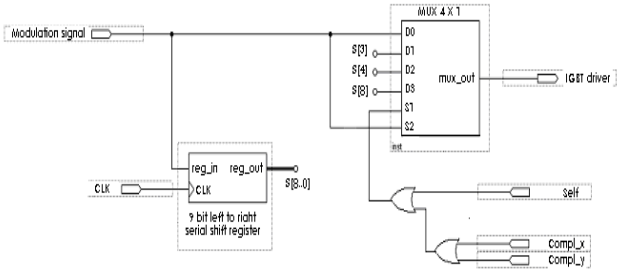

Fig. 9 Control logic for commutation of a single IGBT switch.

The process of commutation from one switch cell to another involves successive change in the status of four IGBT devices in the two commutating switch cells. As the IGBT switches come with their finite switching times, it is essential that sufficient time is provided in between the change of switching status of each switch in order to avoid short-circuit at the input. This is done with the help of a generalized scheme shown in Fig.9 where the logic module for driving any IGBT switch is given. Here, the modulation signal is a binary signal, which gives command to a switch cell to be either on or off. The modulation signal is fed to the input of a 9-bit serial right shift register. The register has

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nine edge triggered D flip-flops in cascade where the output of each flip-flop can be accessed. These flip-flops are used to set the delay required between each IGBT switching transitions. The switching delays have been set on the basis of the type of IGBTs. The turn-on delay of IGBTs of this module is 90 ns and the rise time is 45 ns. The turn-off delay time is 520 ns and fall time is 90 ns.[9]. All the delays are given on the basis of inductive load. Accordingly a total delay of 160 ns for turning on an IGBT switch and 640 ns during turning off has been set. The four step commutation process requires a total time of 1.6 µs (2 x 160 ns + 2 x 640 ns). Hence, a total time interval of 1.6 µs is set aside for safe commutation. The time period of the synchronization clock for the commutation process is set to 160 ns. The status of modulation signal and other signals from sensors etc are periodically monitored at an interval of 1.6 µs. The high going edge of a programmatically generated periodic signal, MSIG_ENA indicates the beginning of the commutation process as shown in Fig.10. The interval between two consecutive high going edges of this signal is 1.6 µs. If the modulation signals' status changes in between this interval, the existing commutation process will not be disturbed and a new process will start at the instant when MSIG_ENA goes high next time. This is necessary as, if a commutation process is interrupted in the middle due to a change in the instantaneous value of modulation signals; it might lead to erroneous commutation and might even violate the switching constraints.

Whenever there is a change in the modulation signal, at the instant MSIG_ENA goes high, the new value of the modulation signal first arrives at input of the 4x1 Mux marked_D0 (Fig.10). At the same instant the signal appears at the input of the first flip-flop in the shift register. The S[3], S[4] and S[8] notations in Fig.10 denotes the output of the fourth, fifth and ninth flip-flop respectively in the register, which are fed to the D1,D2 and D3 input of the 4×1 multiplexer (Mux.) Therefore, any new signal at the input of the register reaches the MUX inputs D1, D2 and D3 after four clock cycles, five clock cycle and nine clock cycles respectively.

A "high" modulation signal status for a bi-directional switch means that in the steady state gate pulses have to be provided to both the IGBT switches of that bi-directional switch cell. The instant, at which each switch will be turned on, will however be different and it depends on the state of the modulating signal and the current direction status of the commutating cells at that instant. The modulation signal sets the least significant control bit (S0) of the MUX while the most significant control bit (S1) is controlled by a combinational logic of the instantaneous current carrying status of relevant IGBT switches. In this figure, 'Self' indicates the current carrying status of the IGBT switch whose gate will be driven by the output signal of the MUX in question and 'Compl x' and 'Compl y' are the current carrying status of the two IGBT switches in the two other bi-directional cell of the same block, which can support current flow in the reverse direction. As an example, for block of switch [S_{11}, S_{12} S_{13}] in Fig.3.10 the timing diagram for commutation from S_{11} to S_{12} when current is flowing from source to load is shown in Fig.3.12.MOD_S_{11} , MOD_S_{12} and MOD_S_{13} are the modulation signals for S_{11}, S_{12} and S_{13} respectively. The t_a and t_b symbols in the figure represent time intervals of 640 ns (four clock periods) and 160 ns(one clock period) respectively. "Current carrying status "1" indicates that the concerned IGBT is conducting and a status "0" indicates that it is not conducting just before the start of commutation i.e. at steady state. We consider here that the switch cell S_{11} will be the outgoing cell and the switch cell S_{12} to be the incoming cell after commutation (Fig.1). Further, we analyze here the transition of the status of IGBT S_{11F} (Fig.1). The direction of the current indicates that before commutation, the IGBT S_{11F} (Fig.1) was conducting; therefore its current carrying status is "1". On similar ground, the current carrying status of IGBT S_{11R} is "0", the current carrying status of IGBT S_{12F} is "0", the current carrying status of IGBT S_{12R} is "0", the current carrying status of IGBT S_{13F} is "0" and the current carrying status of IGBT S_{13F} is "0". Therefore, S1 input (MSB) of MUX is logic "1" and S2 input (LSB) of MUX is logic "0" at the start of commutation process. This ensures that the signal at D2 of the 4X1 MUX is transferred to the output. D2 is connected to the input S[4] and hence the new modulation signal will be effective after the delay of five clock intervals. This will result in the IGBT driver signal for S_{11F} remaining high (value of the modulation signal prior to the start of commutation) for up to five clock (t_a + t_b) periods after the initiation of commutation and then it will go low. This is illustrated in Fig10.

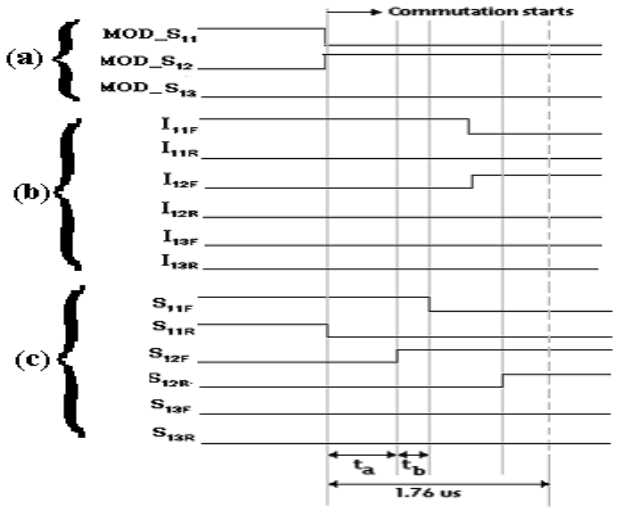

Fig.10. Commutation from S_{11} to S_{12} (a) Modulation signals, (b) current flow information and (c) gate signals to the IGBTs

In the case of a 3x3 phase circuit, where there will be three blocks, the commutation will involve switching transitions between the switch cells belonging to the same block. For instance current flowing in S11 can change over to S12 or S13 without affecting the commutation process in the other two blocks. Hence, these blocks can operate independently of each other.

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VI. SIMULATION RESULTS

The MATLAB Simulation results of four-step and three-step current commutation are shown in Fig.11 and Fig.12 for output current direction is towards load as shown in Fig.5. As soon as there is a change in modulation signal, the gate pulses of the respective IGBTs are generated to facilitate four step commutations. There is no problem of input short circuit and output open circuit as evident from the simulation result.

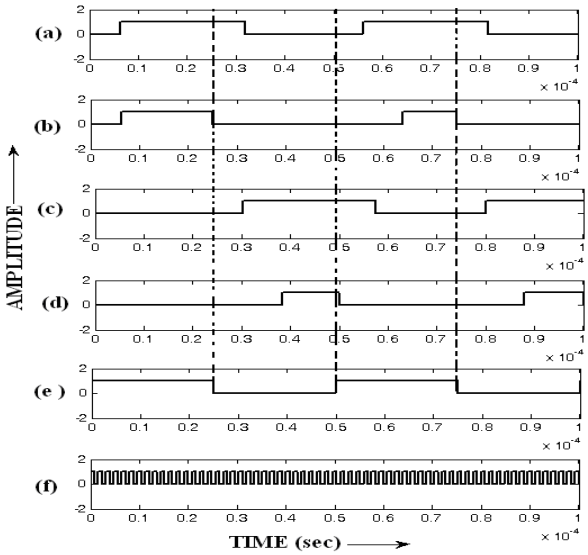

Fig.11(a). Four step commutation: Gating pulses (a) gate signal for the outgoing IGBT 1F in switch cell1, (b) gate signal for the outgoing IGBT 1R in switch cell 1, (c) gate signal for the incoming IGBT 2F in switch cell2, (d) gate signal for the incoming IGBT 2R in switch cell2 and (e) modulation signal for the switch cell 1, (f) clock input for the shift register]=

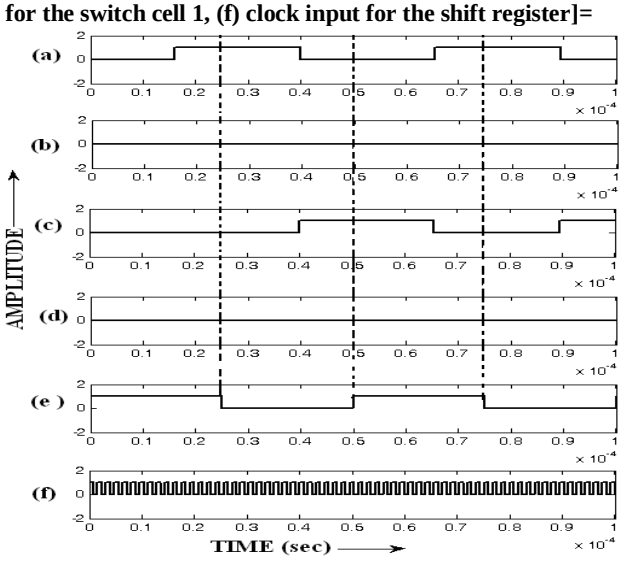

Fig. 11(b): Four step commutation (current carrying status): (a) status signal of forward conducting IGBT (1F) in switch cell 1, (b) status signal of reverse conducting IGBT (1R) in switch cell 1, (c) status signal of forward conducting IGBT (2F) in switch cell2, (d) status signal of reverse conducting IGBT(2R) in switch cell 2, (e) Modulation signal, (f) clock input signal to the shift register

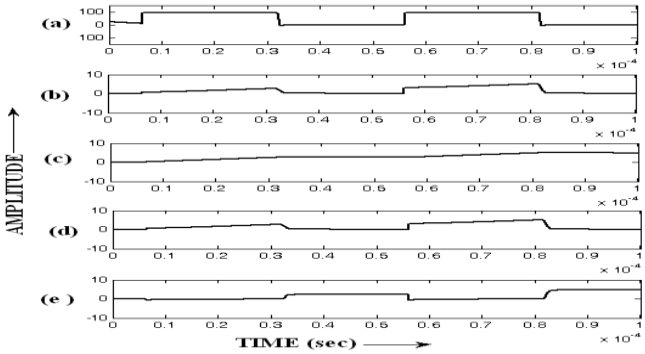

Fig. 11(c): Four step commutation (voltage and current in different parts): (a) Output load voltage across the R-L branch, (b) current flowing in the input supply line connected to switch cell 1, (c) current flowing in the R-L branch, (d) current flowing through Switch cell 1, (e) current flowing through switch cell 2

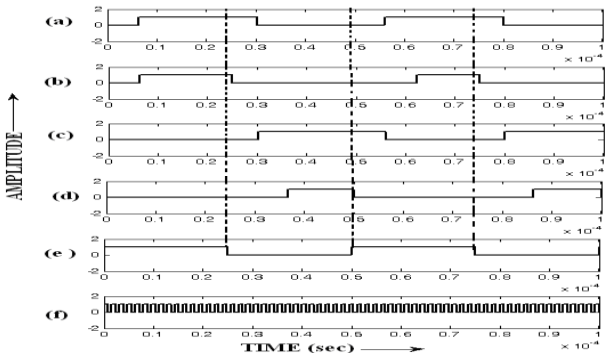

Fig. 12(a). Three step commutation: Gating pulses (a) gate signal for the outgoing IGBT 1F in switch cell1, (b) gate signal for the outgoing IGBT 1R in switch cell 1, (c) gate signal for the incoming IGBT 2F in switch cell2 , (d) gate signal for the incoming IGBT 2R in switch cell2 and (e) modulation signal for the switch cell 1, (f) clock input for the shift register

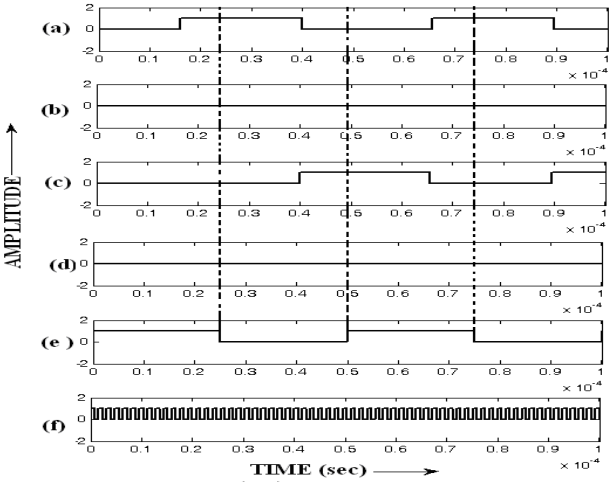

Fig.12(b): Three step commutation (current carrying status): (a) status signal of forward conducting IGBT (1F) in switch cell 1, (b) status signal of reverse conducting IGBT (1R) in switch cell 1, (c) status signal of forward conducting IGBT (2F) in switch cell2, (d) status signal of reverse conducting IGBT(2R) in switch cell 2, (e) Modulation signal, (f) clock input signal to the shift register

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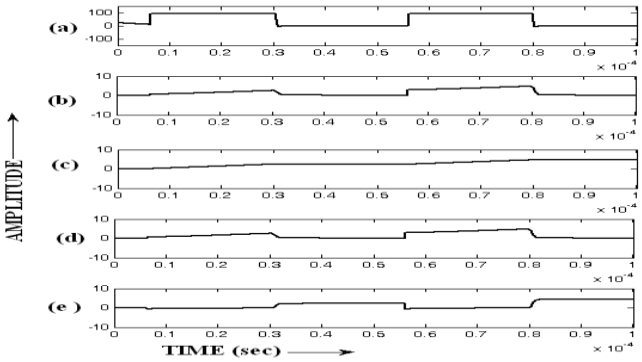

Fig.12 (c): Three step commutation (voltage and current in different parts): (a) Output load voltage across the R-L branch, (b) current flowing in the input supply line connected to switch cell 1, (c) current flowing in the R-L branch, (d) current flowing through Switch cell 1, (e) current flowing through Switch cell 2

VII. CONCLUSION

In this paper, a generalized and synchronous implementation of a widely used current commutation strategy in matrix converter through MATLAB simulink is presented. Output Current based different commutation techniques are studied in depth. The reduction of input short circuit current, output voltage overshoot and commutation intervals are the major objectives of the commutation techniques. This has been observed that even with the Four Step commutation technique, input short circuit current can flow. The reason behind is explained. Near zero current the commutation scheme can fail, causing output voltage notches.

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