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A Two-Stage Class E High-Voltage Ultrasound Pulser for Medical Imaging Applications

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***Abstract*—This paper investigates a Class E high-voltage (HV) pulse generator which can be employed in a front-end transducer for MEMS ultrasound medical imaging applications. Experimental IC measurement results demonstrate that the proposed two-stage configuration provides over 19-V high voltage pulses from 2.5-V and 3-V supply voltages with a 2-Vpp low input triggering signal while maintaining high power efficiencies at a broad range of output loads for 33-MHz MEMS ultrasound transducer.**

***Index Terms*—Class E, ultrasound, MEMS transducer, high voltage pulse generator.**

I. INTRODUCTION

Due to the advantages over the conventional piezoelectric transducer, the capacitive micro-machined ultrasound transducer (CMUT) technology has become an important alternative with the progress of silicon-micromachining techniques [1]. Compared with two-dimensional ultrasound imaging, three-dimensional ultrasound imaging provides more advantages in clinical applications. Moreover, three-dimensional ultrasound potentially tends to be less expensive and less difficult in many areas. On the other hand, three-dimensional imaging systems can form two-dimensional image planes in any orientation relative to the ultrasound transducer array and can acquire volumetric images [1]-[2]. In terms of the state-of-the-art technologies, it is complicated to achieve three-dimensional systems just with a simple method and require a certain degree of capital investments whereas due to the progress of integrated circuit (IC) technologies, the two-dimensional transducer array can reach the same capability of three-dimensional systems. Fig. 1 shows the system functional block diagram of three-dimensional ultrasound imaging systems. By employing more and more elements of IC with transducer arrays can reduce the cost of three-dimensional imaging systems. Each of the front-end interface circuitry includes a driver, a protection scheme, and a readout circuit. Notice that the principal advantage of IC pulse generators (pulsers) is that they can provide high-voltage pulses to each of the elements in the array without large external electronics or a large amount of cables. The inevitable issues [3] associated with two-dimensional array transducers are the increased element count and limited element size in both dimensions due to aperture sampling requirements, which push the requirement of replacing the external wires with the electrical interconnections since excessive interconnections will result in difficulties in implementation.

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Moreover, the limited size severely degrades the element sensitivity. The parasitic capacitances of the limited elements associated with the interconnect lines are of an order of magnitude larger than the transducer capacitances and therefore, large routing capacitances can significantly reduce the output signal amplitude. To discuss these issues, the conventional wiring and routing techniques are required to be further enhanced in order to interface the transducer elements with the driver/readout electronics. Therefore, the integration of the transducer elements with the front-end electronics plays an important role.

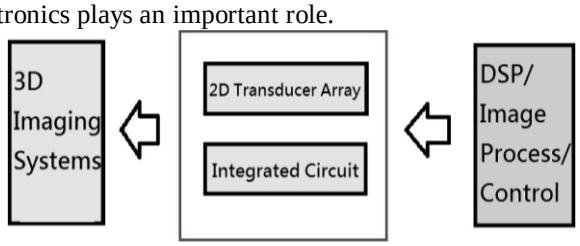

Fig. 1 System diagram of 3D ultrasound imaging systems

In this paper, we propose a high-voltage pulser with a standard IC manufacturing process in order to achieve compact density, thereby increasing package density. Many circuits were also proposed to generate the required high DC voltages [4]. Some of these were based on coupled inductors to achieve the high-voltage gain, others were based on capacitor chains interconnected by diodes and coupled in parallel with two non-overlapping clocks. Moreover, electromagnetic transformers were also developed to generate the required high-voltage pulses. Recent research indicated that the maximum DC voltage produced by the on-chip high-voltage charge pump in silicon-on-insulator CMOS was 27V. These papers presented the technology that can be used in the process of circuit operating at voltages high than 30V in the future [5]-[7].

An approach for rearranging two-dimensional CMUT arrays can be developed by integrating an analog signal preprocessing block beneath each CMUT cell with the aid of vertical connection technologies such as flip-chip bonding [8]-[9] and CMUT-on-CMOS. The capacitive micro-machined ultrasound transducer (CMUT) on the front-end integrated circuit is shown in Fig. 2. The techniques of flip-chip bonding play a role beneath the array because the CMUT consists of a suspended membrane built on a circuit [3]. The CMUT is operated using electrostatic forces: an applied DC bias voltage makes the membrane deflect toward the circuit, while an AC pulse imposed on the bias voltage makes the membrane vibrate, coupling acoustic power to the surrounding medium. When it is employed for reception, the incident acoustic field changes the device capacitance, which

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can employ digital signal to detect the pulse for precise medical imaging calculation.

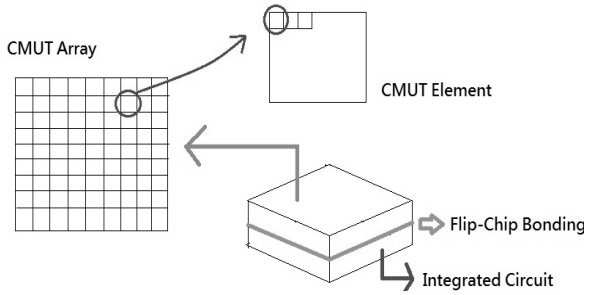

Fig.2 Diagram of a two-dimensional CMUT array integrated with front-end circuit

Due to the low electro-mechanical conversion efficiency, the received signals of present high-frequency ultrasound transducers are required to be amplified and the preamplifier requires protection scheme against the high transmit voltages and immunity from the high-voltage pulse. A regular approach for the traditional protection circuit has an expander/limiter scheme [10]-[11]. The crossed diodes act as switches which are closed (conducting) for large signals (higher than 0.5 V) and open (non-conducting) for small signals. Using two pairs of crossed diodes and a suitable cable length, a simple protection circuit is possible through the diode bridge [11]-[12]. The expander is a diode bridge placed in series with the transmitter circuit that can also make it isolate from the MEMS component and the receiver circuit during the receive mode. Conversely, the limiter is a diode bridge placed in parallel with the receiver circuit and shut the transmitter current at the input of the receiver circuit during the transmit mode.

A switching protection circuit (SPC) could be used as an alternative approach [13] to replace a voltage limiter. The switching protection circuit was high-voltage MOSEFT switches, which required drivers and level-shifters, rather than crossed diodes to isolate the receive circuit. The employment of switching protection circuit reveals two major problems of the conventional approach, which are resolving the non-linear voltage dependent impedance mismatch and relaxation oscillations and these typically require high-voltage power supplies.

A popular approach to implement pulse generator is employing a Class D output stage with a high-voltage manufacturing process. Note that under this principle, not only high-voltage supplies are needed but also complementary high-voltage triggering signals and other high-voltage input control signals are also required. Moreover, since high-voltage signals are spreading almost all the circuits, it compulsively necessitates to employ protection circuitry to prevent short-circuit large currents. In this paper, in order to achieve the targets of high-voltage and high-power-efficiency for front-end transducers, we employ Class E output stages and use shielded choke inductors to boost the output pulse voltage levels with low supply voltages.

To the best of our knowledge, this is the first time that the Class E output stages are announced to be employed as high-voltage ultrasound pulsers for medical imaging applications. In the rest parts of the paper, the high-voltage Class E CMOS front-end pulser is presented in Section II. The verification of the proposed circuit is addressed in Section III and the conclusion is given in the final section.

II. THE PROPOSED TWO-STAGE CLASS E HIGH-VOLTAGE OUTPUT STAGE

The idea behind the Class E output stage operation is to employ the characteristic of non-overlapping output voltage and output current. Under this principle, Class E output stages have the characteristics of high power efficiency, simplicity, and relatively high tolerance to circuit variations.

A. Principles of the Class E Circuit Operation

A general configuration of the Class E output stage is shown in Fig. 3, which it consists of a single supply voltage V_{DD}, a choke inductor L_{dc}, a switch with a parallel capacitor C_p, an optional resonator L_0-C_0, and an output load R_L.

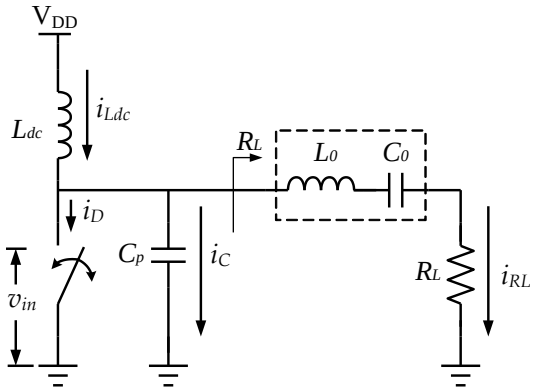

Fig. 3 General configuration of the Class E output stage

The switch is turned on and off periodically at the input frequency. L_0-C_0 resonating at the input frequency is employed if a sinusoidal current is required to the output load R_L. C_p ensures that in the time when the switch is turned off the voltage across the switch still keeps relatively low until after the drain current has reduced to zero. The switch usually uses an active device such as a silicon bipolar transistor or a FET. Note that in order to make the switch near ideal and conduct a higher current, the transistor is designed with a FET of large gate width. The well-known Class E switching conditions [14] include:

1). Voltage return to zero at the switch turn-on: This ensures that the voltage of the switch and the current flowing through it cannot happen simultaneously, and thereby the power dissipation in the switch is zero.

2). Zero voltage slope at the switch turn-on: Although the former point can be satisfied with proper circuit design. The condition of slight mistuning of the amplifier may happen.

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This point can prevent severe power loss at the transient point.

Based on the Class E switching conditions, the ideal Class E voltage and current waveforms can be illustrated in Fig. 4. t_1 and t_2 represent the periods of switch closed and open, respectively. During t_1 period, v_{DS} is zero whereas during t_2 period the current i_D is zero. Because of the characteristic of non-overlap of the current and the voltage, the power dissipation of the switch is zero.

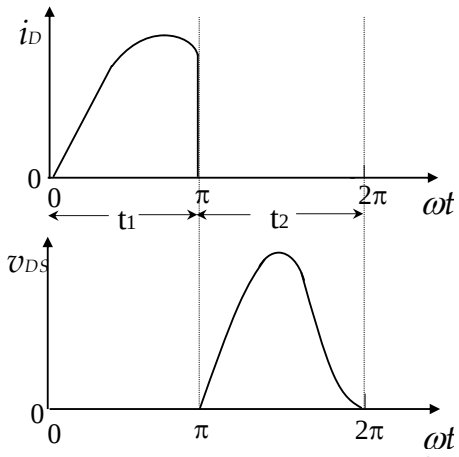

Fig. 4 Ideal Class E voltage and current waveforms

The current equation of the circuit shown in Fig. 3 can be described as

$$i_{Ldc}(t) - i_{RL}(t) = i_D(t) + i_C(t) \quad (1)$$

in which $i_{RL}(t)$ do not necessitate to be sinusoid. To approach ideal Class E switching conditions, in practice there is a relationship between some circuit component values [15], which can be described with the following equation,

$$L_{dc} \approx \frac{0.7436}{\omega^2 C_p} \quad (2)$$

Note that the equation also gives the guideline to determine the values of the choke inductance and the parallel capacitance.

B. The Two-Stage Class E High-Voltage Pulser

The design objective of the proposed circuit is to generate high-voltage pulses with a low supply voltage and a low input trigger voltage while operating at around several tens megahertz and keeping low power consumption. On the other hand, due to the requirement of high-voltage output, the active device must tolerate the high voltage operation. Therefore, the implementation of the proposed pulser circuit is based on the TSMC 0.25-μm CMOS high-voltage mixed-signal general purpose manufacturing process (T25HVG2), which the process provides maximum 60V of drain-to-gate and drain-to-source voltages while the gate-to-source voltage can stand up to 12V. With the provided benefits, we propose the two-stage Class E high-voltage pulser to generate high- voltage pulses for the front-end transmitter to interface two-dimensional CMUTs for ultrasound medical imaging applications.

Fig. 5 shows the proposed Class E high-voltage pulser circuits. The supply voltage of the driver stage V_{DD1} is only 2.5V with the input trigger signal of 2V. M_1 is the switching MOSFET operating at the frequency of input triggering signal v_{IN}, C_{p1} is the parallel capacitor, and L_{dc1} is the shielded choke inductor. Resistor R_1 provides the DC path for the driver stage. Nevertheless, M_1, C_{p1}, and L_{dc1} have to satisfy the Class E operation. By contrast, the supply voltage of the output stage V_{DD2} is 3V, which provides the current to the output load R_L with the switching MOSFET M_2 via shielded choke inductor L_{dc2}. Notice that the switching operation of M_2, L_{dc2}, C_{p2} is also required to meet the Class E switching conditions. If the load resistance R_L is not matched to the optimum load, the matching network is required to insert between C_{p2} and R_L in order to obtain the maximum drain voltage of M_2. The transformed optimum load via the inserted matching network increases with an increase of the supply voltage [16].

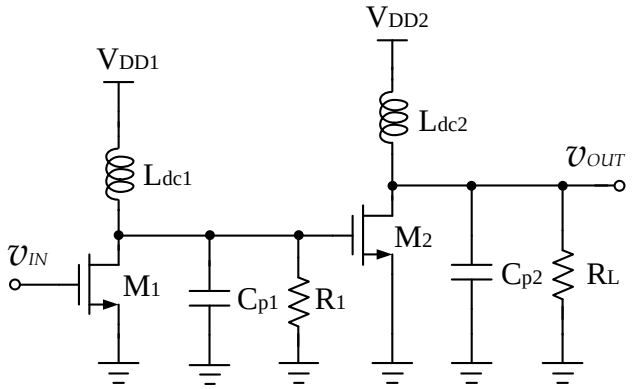

Fig. 5 Schematic diagram of the proposed two-stage Class E high-voltage pulser

The rising and falling slopes of the output voltage pulse can be investigated with the following voltage and current equations of the second stage when the transistor M_2 is off,

$$L_{dc2} \frac{di_{Ldc2}(t)}{dt} = V_{DD2} - v_{DS2}(t) \quad (3)$$

$$C_{p2} \frac{dv_{DS2}(t)}{dt} = i_{Ldc2}(t) - \frac{v_{DS2}(t)}{R_L} \quad (4)$$

The rising slope of the output voltage pulse at the period of $\pi/\omega \le t \le 3\pi/2\omega$ can be obtained with the boundary condition and the minimum switching power loss at $t=\pi/\omega$ [17], which yields

$$v_{DS}\left(\frac{\pi}{\omega}\right) = 0 \quad (5)$$

$$\left.\frac{dv_{DS}(t)}{dt}\right|_{t=\frac{\pi}{\omega}} = 0 \quad (6)$$

by substituting $L_{dc2}C_{p2}$ with $0.7436/\omega^2$ according to the relationship indicated in equation (2), we can obtain the

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slope of the voltage pulse $dv_{DS}(t)/dt$ at the period of transistor off $\pi/\omega \le t \le 3\pi/2\omega$ as follows,

$$\frac{dv_{DS}(t)}{dt} \approx -V_{DD}\omega \sin \omega t \quad (7)$$

On the other hand, with the Class E switching conditions of equations (8) and (9)

$$v_{DS}\left(\frac{2\pi}{\omega}\right) = 0 \quad (8)$$

$$\left.\frac{dv_{DS}(t)}{dt}\right|_{t=\frac{2\pi}{\omega}} = 0 \quad (9)$$

We can obtain the falling slope of the voltage pulse $dv_{DS}(t)/dt$ at the period of transistor off $3\pi/2\omega \le t \le 2\pi/\omega$ as follows,

$$\frac{dv_{DS}(t)}{dt} \approx V_{DD}\omega \sin \omega t \quad (10)$$

Obviously, equations (7) and (10) indicate that the absolute values of rising and falling slopes increase with an increase of the supply voltage V_{DD} or the operating frequency.

III. EXPERIMENTAL AND MEASURED RESULTS

In order to validate the proposed Class E high-voltage pulser, the prototype test IC experiment has been performed. The implementation of the proposed pulser circuit is based on the devices which can provide at least 30V of drain-to-gate and drain-to-source voltages while the gate-to-source voltage can stand up to 12V. Therefore, we implement the circuits in the TSMC 0.25μm CMOS high-voltage technology process provided through the CIC service (TSMC T25HVG2 manufacturing process).

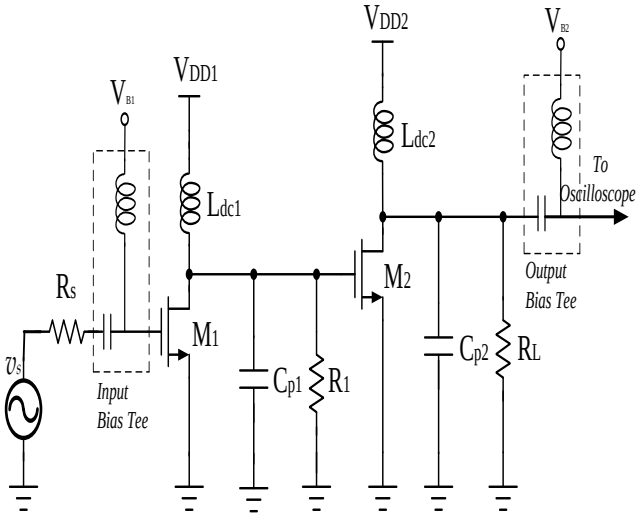

Fig.6 Complete schematic for measurement of the proposed IC pulser including off-chip passive devices

The complete schematic for the measurement of the pulser is shown in Fig. 6 including the off-chip passive components. Note that since the loads can be varied, we also mounted a resistor and a capacitor on the test board to investigate the output voltage levels for different combinations of resistive and capacitive output loads.

The die photo of the proposed configuration (active devices only) is shown in Fig. 7. The switching transistors for the pulser are arranged with a multi-finger configuration. The bonded input pad is on the lower left corner of the photo. Other pads are bonded to the test boards which mounted the rest passive devices.

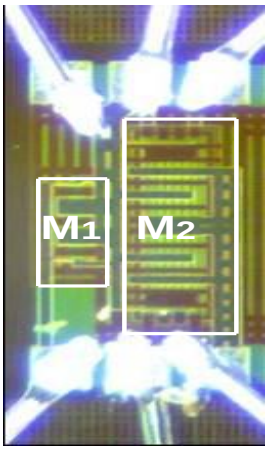

Fig. 7 Die photo of the proposed IC pulser

The die of the proposed IC pulser was mounted on the test board and bonded. The measured output voltage signal waveform for the configuration is shown in Fig. 8 which indicates the measured result of the two-stage configuration, in which a 19.2-Vpp output signal level can be obtained at approximately 33MHz operating frequency under the condition of a 2-Vpp input triggering signal and 2.5-V and 3-V supply voltages for the first stage and second stage, respectively.

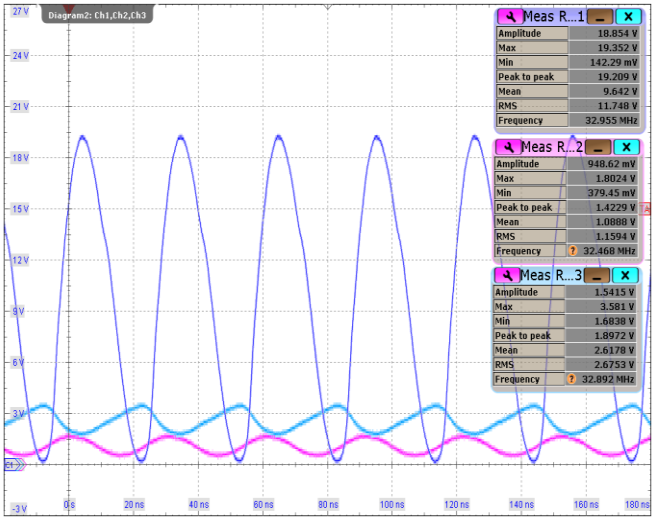

Fig. 8 Measured output signal waveforms for the two-stage IC pulser

The power efficiency and output peak voltage level have also been investigated for both configurations. Obviously, over 70% power efficiencies at a broad range of output

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resistive loads are indicated in Fig. 9. The influences of the capacitive load on the output peak voltage level and power efficiency have also been explored as indicated in Fig. 10. Notice that the variation of output capacitance has been tuned together with the choke inductance and under this experimental condition, the power efficiency can be maintained for a broad range of output capacitive loads as indicated in Fig. 10. Performance characteristics of the implemented IC are summarized in Table I.

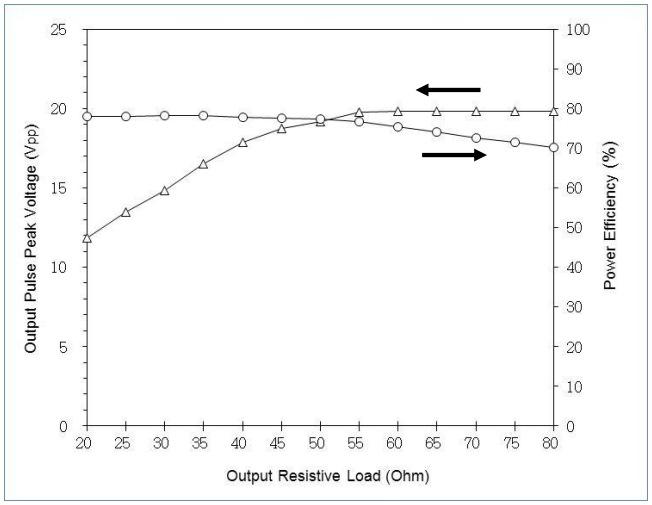

Fig.9 Measured peak voltage level of output signal and power efficiency versus output resistive load

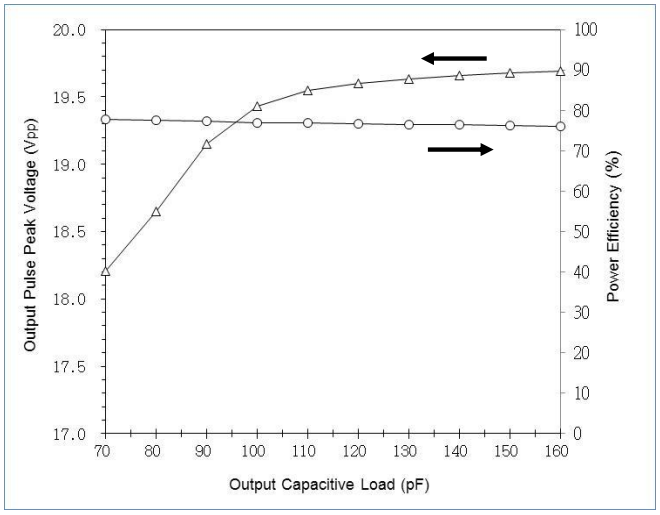

Fig.10 Measured peak voltage level of output signal and power efficiency versus output capacitive load

TABLE I. PERFORMANCE SUMMARY OF THE IC PULSER

Technology	TSMC 0.25μm, High-Voltage CMOS
Supply voltage(s)	2.5V and 3V
Output voltage	$19.2V_{pp}$
Operating frequency	33MHz
Output capacitive load	70-160pF
Output resistive load	20-80Ω
Active die size	$0.750\times0.708mm^2$

IV. CONCLUSION

A newly proposed Class E high-voltage ultrasound pulser for front-end transmitters to interface two-dimensional CMUTs has been presented. With the inherent characteristics of the Class E operation, the proposed alternative implementation approach has the benefits of low supply voltage, high output voltage level, high power efficiency, and do not have the conventional large short-current problem and its protection circuit overheads.

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