

FPGA Based Implementation of Pulse Position Modulation for Underwater Optical Wireless Communication

Rabee M. Hagem

¹Centre for Wireless Monitoring and Applications, School of Electronic Engineering, Griffith University, Brisbane/Queensland/Australia

²Sports and Biomedical Engineering Lab (SABEL), School of Electronic Engineering, Griffith University, Brisbane/Queensland/Australia

³University of Mosul/ College of Engineering/ Computer Engineering Department

Abstract— *The popular modulations approaches used in underwater optical wireless communication systems are on-off keying and PPM (Pulse Position Modulation). This paper presents the implementation of the PPM modulation based on FPGA. The modulation and demodulation are achieved using the Altium Nano Board 3000 (provided with Spartan 3AN FPGA) at the transmitter and the receiver. A mixed design of schematic capture and a VHDL code where adapted to generate the required modulation schemes. The simulation results showed that the design perform the implemented algorithm at a performance speed of 160 MHz which is suitable for optical communications.*

Index Terms— FPGA, PPM modulation and demodulation Underwater optical wireless communication, VHDL.

I. INTRODUCTION

Underwater optical wireless communication (UOWC) is used as an alternative effective solution compared with acoustic and Radio frequency (RF) communication. It is the best to use in applications that need high data rate transferring in short time which reduce the power consumption such as videos and pictures that are fundamentals for data surveillance and monitoring. Low power, low cost, small size and high data rate Gb/s that the sensor have based on optical wireless communication paved the way to use this technology in underwater wireless sensor networks (UWSNs). Optical wireless communication is used in underwater environment due to the growing need of reliable system for monitoring and observation [1]. The green/blue region is popular to be used because of the low attenuation in this range. In addition, the high data rate compared with the acoustic that has low speed (1500m/s) with low data rate and high power consumption or the electromagnetic waves that has very high attenuation due to the high frequency. The optical wireless communication is usually achieved using light emitting diode (LED) as a light source or laser and a photodetector as a receiver. The important part of the optical wireless communication is choosing the modulation technique that is required to achieve a reliable communication [2]. This paper presents a PPM modulator and demodulator based on Altium Nanoboard 3000 that is provided with Spartan 3AN FPGA. The paper is

organized as: In section II, the modulation techniques that are used in optical wireless communication are outlined. Section III presents and describes the proposed system design taking into account the design concepts. Design implementation, results and discussion are presented in section IV. Conclusion and future development appear in section V.

II. MODULATION TECHNIQUES IN OPTICAL WIRELESS COMMUNICATION

The basic modulation techniques are Frequency modulation (FM), Amplitude modulation (AM) and Phase modulation (PM). In Amplitude shift keying (ASK), the digital data is represented based on the variations in the carrier wave amplitude and this depends on the bit stream (modulating signal). In optical wireless communication (IM/DD) (Intensity modulation /direct detection) and ON-OFF keying (OOK) is used due to the low cost and less complexity in implementation.

The embedded systems that are used in underwater environment should be small size, light weight as much as possible and use batteries because the power consumption is very important factor. PPM has low complexity implementation and can transmit data for long distance [3].

PPM is used for underwater optical wireless communication because of the low transmitting power consumption and better anti-noise performance compared with other modulation techniques. The drawback of the PPM technique is the low bandwidth presented makes it not the best in sending large amount of data [4].

In PPM, the M message bits which represent the transmitted data are encoded in order to transmit a single pulse in one of 2^M possible time shift. At each time interval T_s , $L=2^M$ time shift constitute a PPM frame.

The time slot or PPM pulse transmit optically. At the receiver, the photo detector detects the light pulses and according to their time slots, a decision algorithm is applied to recover the original information [4]. Fig (1) shows the Bit Error Rate (BER) with Signal to Noise Ratio (SNR) for different modulation techniques [3].

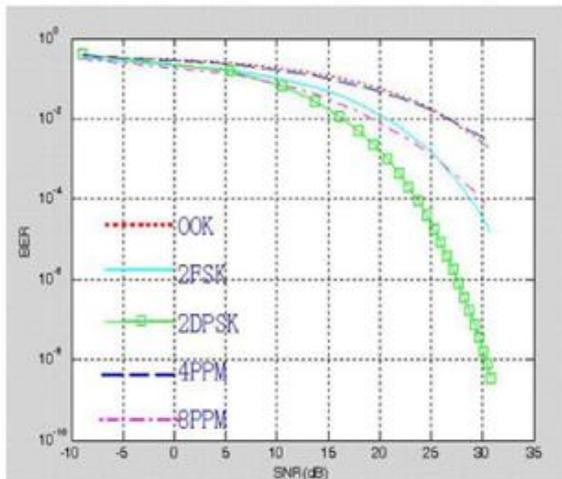


Fig. (1): BER with SNR for different modulation techniques [3].

PPM modulation technique has received a wide attention in the last decade and the research has been extended into various forms, such as single-pulse position modulation (L-PPM), differential pulse position modulation (DPPM), digital pulse interval modulation (DPIM), multi-pulse position modulation (MPPM), overlapping pulse position modulation (OPPM), pulse rate modulation (APPM), shorten pulse position modulation (SPPM), pulse interval modulation (PIM), and polarized differential pulse interval modulation (P-DPIM). All of these modulation techniques are based on PPM and the main goals of the modified PPM are to improve the bit error rate, power consumption by making them lower and increase the data rate and bandwidth [3-5]. Table I shows the performance for the PPM and the modified PPM [4].

Table I: Performance of PPM and the modified PPM [4].

Modulation mode	Average demand for bandwidth (bit/s)	Average power demand in transmitter	Channel capacity (bits/symbol)
PPM	$\frac{2^M}{M} R_b$	$\frac{1}{2^M} P_t$	N
DPPM	$\frac{2^M + 1}{2^M} R_b$	$\frac{2}{2^M + 1} P_t$	$N 2^{(M+1)} / (2^{M+1})$
DH-PIM	$\frac{2^M - 1 + 5}{2^M} R_b$	$\frac{3}{2^M - 1 + 5} P_t$	$N 2^{(M+1)} / (2^{M-1+5})$
SPPM	$\frac{2^M - 1 + 1}{M} R_b$	$\frac{3}{2^M + 2} P_t$	$N 2^{(M+1)} / (2^{M+2})$

Where R_b represents the information transmission rate and P_t represents the power required when “1” pulse is sent. Fig (2) shows the implementation of the SPPM which is the same for the PPM. The only difference is the SPPM is represented by one bit less.

The main procedure for the PPM is by transforming the serial data to parallel, then applying the PPM modulation algorithm. The data is sent through the underwater optical wireless channel. Then by using serial to parallel to transform the data to serial after passing the optical detector and the

PPM demodulation to recover the original data back [4].

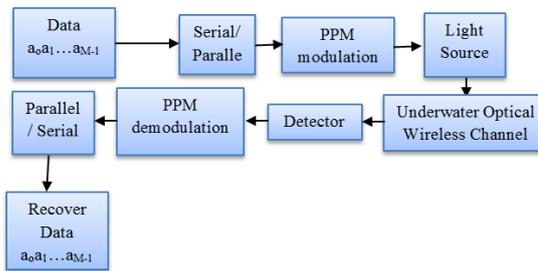


Fig. (2): The principle of PPM modulation [4].

The PPM or one of the modified PPM is the best to use in underwater environment. Smart transmitter and receiver and digital video streaming where designed and implemented based on optical wireless communication with different modulation techniques for underwater applications [6-9]. This paper focused on implementing the PPM modulator and demodulator; however, the modified PPM modulation can be implemented as well [4].

III. THE PROPOSED SYSTEM DESIGN

The proposed PPM circuit contains the digital blocks of data generator, the PPM modulator and the PPM demodulator. The data generator circuit generates a pseudo code to test the PPM circuit. Four serially-connected registers with an EX-OR gate between the first and last register to feed the first register and to generate a different bit at each clock pulse. The registers are initialized with logic ‘1’ through the preset pin otherwise the generated output would keep holding ‘0’ at each clock pulse.

The data generator is connected to the PPM circuit as the block diagram presented in Fig. (3).

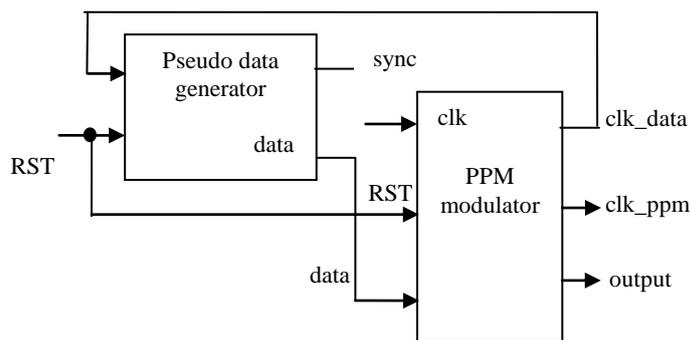


Fig. (3): The code-generator and the PPM block diagram

The clock generator has two inputs (the clock and reset), the clock is provided by the PPM block and the reset is used to initialize the registers; and two outputs (the generated data and the synchronization output). The generated data is connected to the PPM input whereas the sync is used as a synchronization signal that give logic ‘1’ when all registers hold ‘1’.

In our design, the number of bits (M)= 4 and the number of chips or pulses (L)= 2^M = 16. In this case, the design requires 3 different rates of clock, the main clock; the data generated

clock and the PPM clock. The relation between these clocks is as follows:

$$\text{PPM clock} = \text{main clock}/2$$

$$\text{Data generator clock} = \text{main clock}/32 = \text{PPM clock}/16$$

The main clock of the design is the FPGA clock board which can be set to different rates. Other clock rates can be derived from the main clock using a clock divider through the VHDL code. It is worthwhile to mention that the logic analyzer (LAX) used to capture the signals throughout the design is provided with two clocks, the main clock and the captured one which is usually slower than the main. Fig. (4) shows part from the timing simulation for the blocks in Fig. (3).

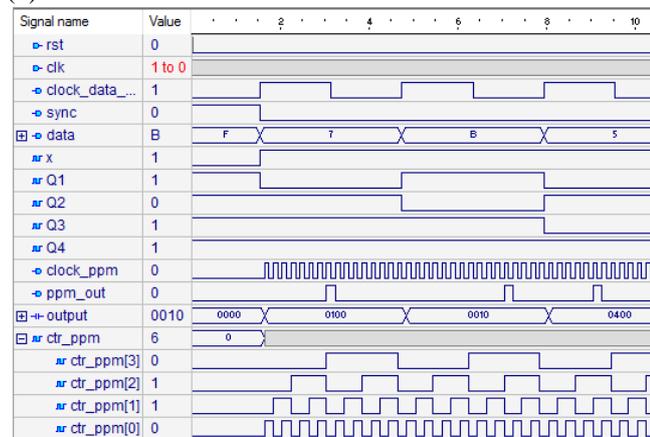


Fig. (4): The timing simulation of the PPM design.

It can be seen from Fig. 4 the input, output and internal signals of the design. The sync out '1' when the data generated is 'F' in hexadecimal indicating all registers hold '1'. Fig. 4 indicates the clocks derived in the design and also shows the data generated individually and in group as well. The ppm_out signal shows the decoding of the input data where the pulse takes different positions according to the input data.

IV. DESIGN IMPLEMENTATION

The PPM design is implemented on the Spartan 3AN FPGA available on the NanoBoard Altium 3000 presented in Fig. (5) utilizing the Altium designer software package. This board is equipped with many input/output facilities such as ports, switches and pins; and the provided FPGA can be programmed through the system JTAG cable which is also used to measure the FPGA I/O signals [10].



Fig. (5): The NanoBoard 3000

In the Altium designer and under the FPGA project, the design can be created either from VHDL code or schematic capture or both methods in the design sheet. The design sheet shown in Fig. 6 contains the blocks designed with VHDL (green), the necessary delay circuit for FPGA startup and the logic analyzer for signal capture with the required circuitry. These blocks are connected together and the required inputs of clock board and reset are also connected to the design.

The PC to NanoBoard connection is made through the JTAG link which is a well-known IEEE standard chain for programming and testing.

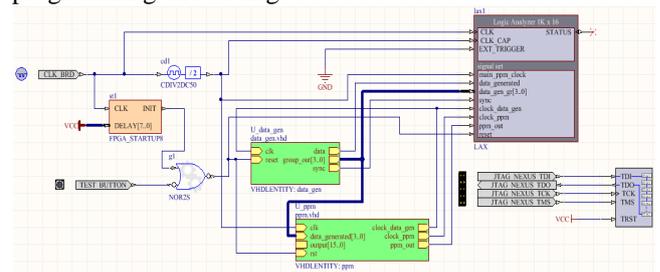


Fig. (6): The FPGA implementation of the PPM design.

The device utilization resources for the PPM design can be seen in Table II where the whole implementation occupies a small portion of the FPGA (XC3S1400AN) resources. These numbers generated post FPGA implementation.

Table II: Device resources- usage summary

I/O pins	6/ 502
Block RAM	1/32
Slice Flip Flops	576/ 22528
Slices	562/ 11264
Total 4-input LUTs-Logic	847/ 22528

The clock rate for the design is 160 MHz and as previously mentioned, the derived clocks from the main clock are the PMM clock of 80 MHz and the data generated clock of $80/16 = 5$ MHz. Low-resource utilization design allows higher clock rates since the critical path (longest propagation delay between two storage elements) is short.

The signal timing for the data generator, PPM and PPM demodulator can be seen in Fig. (7). In this figure, the reconstructed original information is presented.

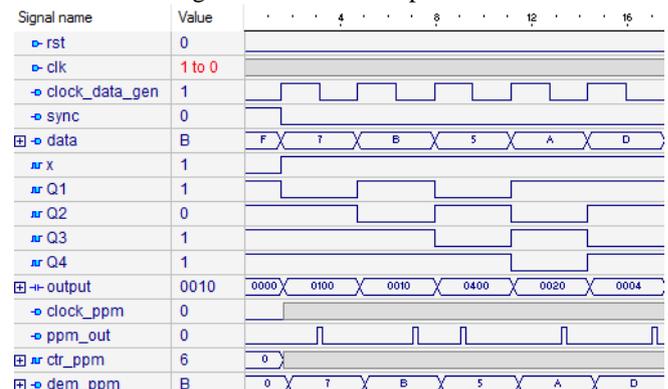


Fig. (7): The main signals in the design.

Fig. (7) Shows the generated information (data), the PPM output (ppm_out) and the reconstructed information (dem_ppm) in which the original information is recovered with few clock pulses (clock_ppm) as a delay. At the first data generator clock pulse, the data (F) is lost due to initialization and generation of clocks, whereas other information sent is recovered at the output signal dem_ppm. The clock (clk) and clock_ppm are compressed here in order to show the lower rate of clock_data_gen in addition to the data sent and the ppm_out.

V. CONCLUSION

The PPM is a highly regarded modulation technique for data transmission in wireless underwater optical communications. As a digital circuit, the PPM can be efficiently implemented on FPGA including all the required blocks of the modulator. With low utilization design resources, the FPGA can be run at high clock rates (160 MHz in this paper) without disrupting the PPM generated, modulated and reconstructed signals. This leads to conclusion that the PPM is highly suitable to be used for underwater optical communications. For future work different modified PPM can be applied and compared.

ACKNOWLEDGMENT

The author wants to thanks Dr. Yahya T. Qassim a member of the Centre for Wireless Monitoring and Applications with Griffith University and also member in the sports and biomedical engineering laboratory (SABEL) for helping and providing great notes with the nano board 3000.

REFERENCES

- [1] R. M. Hagem, S. G. O. Keefe, T. Fickenscher, and D. V. Thiel, "Self-Contained Adaptable Optical Wireless Communications System for Stroke Rate during Swimming," *IEEE Sensors Journal*, vol. 13, pp. 3144-3151, 2013.
- [2] D. Anguita, D. Brizzolara, and G. Parodi, "VHDL modules and circuits for underwater optical wireless communication systems," *WTOC*, vol. 9, pp. 525-552, 2010.
- [3] S. Meihong, Y. Xinsheng, and Z. Fengli, "The Evaluation of Modulation Techniques for Underwater Wireless Optical Communications," in *Communication Software and Networks*, 2009. ICCSN '09, pp. 138-142, 2009.
- [4] S. Meihong, Y. Xinsheng, and Z. Zhangguo, "The Modified PPM Modulation for Underwater Wireless Optical Communication," in *Communication Software and Networks*, 2009. ICCSN '09, pp. 173-177, 2009.
- [5] X. Mi and Y. Dong, "Polarized digital pulse interval modulation for underwater wireless optical communications," in *OCEANS 2016 - Shanghai*, pp. 1-4, 2016.
- [6] M. Doniec, X. Anqi, and D. Rus, "Robust real-time underwater digital video streaming using optical communication," in *Robotics and Automation (ICRA)*, 2013 pp. 5117-5124, 2013.
- [7] M. Doniec, C. Detweiler, I. Vasilescu, and D. Rus, "Using optical communication for remote underwater robot operation,

"in Intelligent Robots and Systems (IROS), 2010 pp. 4017-4022, 2010.

- [8] J. A. Simpson, W. C. Cox, J. R. Krier, B. Cochenour, B. L. Hughes, and J. F. Muth, "5 Mbps optical wireless communication with error correction coding for underwater sensor nodes," in *OCEANS 2010 MTS/IEEE SEATTLE*, pp. 1-4, 2010.
- [9] J. A. Simpson, B. L. Hughes, and J. F. Muth, "Smart Transmitters and Receivers for Underwater Free-Space Optical Communication," *IEEE Journal on Selected Areas in Communications*, vol. 30, pp. 964-974, 2012.
- [10] Altium Limited, "Nanoboard-3000" Accessed Nov. 10, 2016 <http://nb3000.altium.com/intro.html>

AUTHOR BIOGRAPHY



Dr. Rabee M. Hagem received the B.Sc. degree in electronics and communication engineering from Mosul University, Mosul, Iraq, in 1998, and the M.Sc. degree in electronic and communication in 2001. He received a Ph.D degree from Griffith University/ Brisbane/Queensland/Australia in underwater optical wireless communication for real

time swimmers feedback in 2014. He is a member of the Centre for Wireless Monitoring and Applications with Griffith University. He has been a Lecturer with the Computer Engineering Department, Mosul University, since 2003 till now. He was a R&D Engineer for North Mosul Electricity Distribution Company in 2001 and 2002 and as a QA/QC Engineer for ABB Company for extension of Mosul 400 Kv substation project in 2007. His current research interests include underwater optical wireless communication, design and implementation of smart sensors, embedded systems for athletes monitoring, and sport data analysis.