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Performance Analysis of Twenty Seven Level POD Modulation based Cascaded H-Bridge Multi Level Inverter Topology

B.Anusha[1], Dr K.Satyanarayana[2], Ch. V. V. Manga Lakshmi [3]
M. Tech Student, Pragati Engineering College, Surampalem
Professor & HOD-EEE of Pragati Engineering College, Surampalem.
Assist Professor of EEE, Pragati Engg College, Surampalem.

Abstract*— Multi level inverters are suitable of high power handling capacity, associated with lower output harmonics and lower commutation losses. But the main disadvantages of multi level inverters are complexity, requiring a more number of power devices and passive components and complex control circuitry. Hence a Twenty Seven Level Cascaded H-Bridge multi level inverter (CHBMLI) topology is proposed which requires only twelve switches and those switches are controlled by using of New PWM technique i.e., POD (Phase Opposition and Disposition) modulation method whereas 52 switches are required in the conventional cascaded H- bridge multi level inverter (CHBMLI) for twenty seven Level by using of repeating sequence method. The proposed POD based cascaded H- bridge multi level inverter topology offers strong advantages such as improved output waveforms, lower THD and lower electromagnetic interference. Here the performance of an asymmetrical configuration of Twenty Seven-level inverter (TSLI) based Cascaded H-Bridge Multi Level topology with R & RL loads is analyzed and compared with conventional CHBMLI with repeating sequence as switching technique. The performance factors are analyzed with the usage of minimum number of switches so that switching losses can be reduced effectively with proposed cascaded H-bridge multi level approach.

***Index Terms*— CHBMLI, TSLI, Repeating Sequence, Phase opposition disposition (POD), THD.**

I. INTRODUCTION

Since past decade, multilevel inverters have drawn increasing attention because of their promising applications in power systems and industrial drives. They can be efficiently used in the distributed energy systems in which, output ac voltage is obtained by connecting dc sources such as batteries, fuel cells, solar cells, rectified wind turbines etc at input side of the inverters mentioned in [1-2]. The ac output voltage obtained from the inverters can be fed to a load directly or interconnect to the ac grid without voltage balancing problems.

The multilevel inverters offer several advantages as compared to the hard-switched two-level pulse width modulation inverters, such as their capabilities to operate at high voltage with lower dv/dt per switching, high efficiency, low electromagnetic interference etc. High magnitude sinusoidal voltage with extremely low distortion at fundamental frequency can be produced at output with the help of multilevel inverters by connecting sufficient number of dc levels at input side. There are mainly three types of multilevel inverters; these are a) diode- clamped, b) flying capacitor and c) cascade multilevel inverter (CHBMLI). Among these three, CHBMLI has a modular structure and requires least number of components as compared to other two topologies, and as a result, it is widely used for many applications in electrical engineering mentioned in [3-5].

To produce multilevel output ac voltage using different levels of dc inputs, the semiconductor devices must be switched ON and OFF in such a way that the fundamental voltage is obtained as desired along with the elimination of certain number of higher order harmonics in order to have least harmonic distortion in the ac output voltage. For switching the semiconductor devices, proper selection of switching angles is must. The switching angles at fundamental frequency, in general, are obtained from the solution of non linear transcendental equations characterizing harmonics contents in the output ac voltage; these equations are known as selective harmonic elimination (SHE) equations mentioned in [6-10].

A single-phase multi string five-level inverter integrated with an auxiliary circuit was recently proposed for dc/ac power conversion described in [11-12]. This topology used in the power stage offers an important improvement in terms of lower component count and reduced output harmonics. Unfortunately, high switching losses in the additional auxiliary circuit caused the efficiency of the multi string five-level inverter to be approximately 4% less than that of the conventional multi string three-level inverter in [13]. A novel isolated single-phase inverter with generalized zero vectors (GZV) modulation scheme was first presented to simplify the configuration. However, this circuit can still only operate in a limited voltage range for practical applications and suffer degradation in the overall efficiency as the duty cycle of the dc-side switch of the front-end conventional boost converter approaches unity in [13-14]. Furthermore, the use of isolated transformer with multi windings of the GZV based inverter results in the larger size, weight, and additional expense.

The newly constructed inverter topology offer strong advantages such as improved output waveforms, smaller filter size, and lower EMI and total harmonics distortion (THD).

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An asymmetrical configuration of eleven-level inverter (ELI) based Multi String Multi Level topology fed Three Phase Induction Motor Drive performance is analyzed and compared with conventional cascaded H- bridge multi level inverter and the performance factors are obtained at both transient and steady state operating conditions with usage of minimum number of switches so that switching losses can be reduced effectively with multi string multi level approach. Performance Analysis of Eleven Level Asymmetrical Multi String Multi Level Inverter fed Three Phase Induction Motor Drive [15].

II. BASIC MULTI LEVEL INVERTER TOPOLOGIES

1. Basic Five level Cascaded H-Bridge Multi level inverter(CHBMLI)

The Basic circuit of five level Cascaded H-bridge multi level inverter (CHBMLI) with eight switches as shown in Fig.1 and corresponding output voltage waveforms are shown in Fig.2. In this approach, all the eight switches are operated with a switching frequency of 50 Hz and the input voltage of Vdc=100V. The symmetrical multilevel approach of the Cascaded H-bridge inverter is operated with equal voltage values at the input side of the inverter. In a symmetrical Cascaded H-bridge multi level inverter, the Seven, Nine, Eleven and Thirteen levels are generated by using 12,16,20,24 switches respectively with repeating sequence as gating signal. The corresponding Switching states and terminal output voltages of five-level Cascaded H-bridge Multi level inverter is shown in Table .1

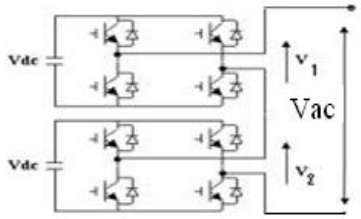

Fig.1: Five level Cascaded H-Bridge inverter

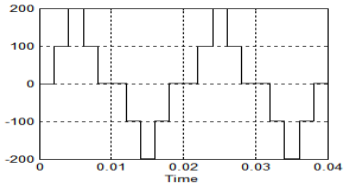

Fig.2: Output voltages of five level CHBMLI

Table.1: Switching states and terminal voltage of five-level CHBMLI

V_O	Swiches in cascaded H-bridge Five level Multi level Inverter							
	S1	S2	S3	S4	S5	S6	S7	S8
+2Vs	1	1	0	0	1	1	0	0
+Vs	1	1	0	0	1	0	1	0
+Vs	1	0	1	0	1	1	0	0
0	1	0	1	0	1	0	1	0
-Vs	0	0	1	1	1	0	1	0
-Vs	1	0	1	0	0	0	1	1
-2Vs	0	0	1	1	0	0	1	1

2. Twenty Seven Level Cascaded H-Bridge Multi level inverter (CHBMLI)

The Twenty seven Level Cascaded Multi level inverter circuit is shown in Fig.3 in a symmetrical approach with an input voltage of 25 V and corresponding output voltage waveforms are shown in Fig.4. It requires 52 switches to get Twenty seven level of output voltage. The Table.2 shows the operation of switches at different levels of voltages.

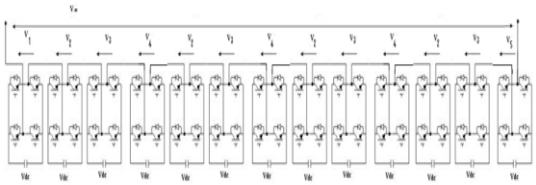

Fig.3: Twenty Seven level CHBMLI

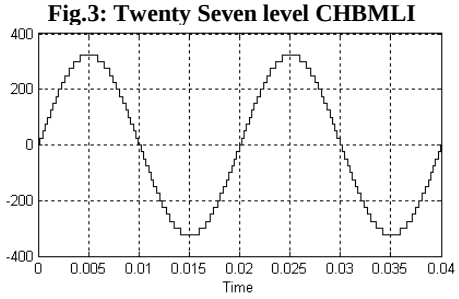

Fig.4. Output voltage of Twenty Seven level conventional CHBMLI

Table 2: Switching states and terminal voltages of twenty seven level CHBMLI with repeating sequence at positive side of segments

V_O	0	+vs	+2vs	+3vs	+4vs	+5vs	+6vs	+7vs	+8vs	+9vs	+10vs	+11vs	+12vs	+13vs
S1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
S2	1	0	0	0	0	0	0	0	0	0	0	0	0	0
S3	0	0	0	0	0	0	0	0	0	0	0	0	0	0
S4	0	1	1	1	1	1	1	1	1	1	1	1	1	1
S5	1	1	1	1	1	1	1	1	1	1	1	1	1	1
S6	1	1	0	0	0	0	0	0	0	0	0	0	0	0
S7	0	0	0	0	0	0	0	0	0	0	0	0	0	0
S8	0	0	1	1	1	1	1	1	1	1	1	1	1	1
S9	1	1	1	1	1	1	1	1	1	1	1	1	1	1
S10	1	1	1	0	0	0	0	0	0	0	0	0	0	0
S11	0	0	0	0	0	0	0	0	0	0	0	0	0	0
S12	0	0	0	1	1	1	1	1	1	1	1	1	1	1
S13	1	1	1	1	1	1	1	1	1	1	1	1	1	1
S14	1	1	1	1	0	0	0	0	0	0	0	0	0	0
S15	0	0	0	0	0	0	0	0	0	0	0	0	0	0
S16	0	0	0	0	1	1	1	1	1	1	1	1	1	1
S17	1	1	1	1	1	1	1	1	1	1	1	1	1	1
S18	1	1	1	1	1	0	0	0	0	0	0	0	0	0
S19	0	0	0	0	0	0	0	0	0	0	0	0	0	0
S20	0	0	0	0	0	1	1	1	1	1	1	1	1	1
S21	1	1	1	1	1	1	1	1	1	1	1	1	1	1
S22	1	1	1	1	1	1	0	0	0	0	0	0	0	0

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S23	0	0	0	0	0	0	0	0	0	0	0	0	0	0
S24	0	0	0	0	0	0	1	1	1	1	1	1	1	1
S25	1	1	1	1	1	1	1	1	1	1	1	1	1	1
S26	1	1	1	1	1	1	1	0	0	0	0	0	0	0
S27	0	0	0	0	0	0	0	0	0	0	0	0	0	0
S28	0	0	0	0	0	0	0	1	1	1	1	1	1	1
S29	1	1	1	1	1	1	1	1	1	1	1	1	1	1
S30	1	1	1	1	1	1	1	1	0	0	0	0	0	0
S31	0	0	0	0	0	0	0	0	0	0	0	0	0	0
S32	0	0	0	0	0	0	0	0	1	1	1	1	1	1
S33	1	1	1	1	1	1	1	1	1	1	1	1	1	1
S34	1	1	1	1	1	1	1	1	1	0	0	0	0	0
S35	0	0	0	0	0	0	0	0	0	0	0	0	0	0
S36	0	0	0	0	0	0	0	0	0	1	1	1	1	1
S37	1	1	1	1	1	1	1	1	1	1	1	1	1	1
S38	1	1	1	1	1	1	1	1	1	1	0	0	0	0
S39	0	0	0	0	0	0	0	0	0	0	0	0	0	0
S40	0	0	0	0	0	0	0	0	0	0	1	1	1	1
S41	1	1	1	1	1	1	1	1	1	1	1	1	1	1
S42	1	1	1	1	1	1	1	1	1	1	1	0	0	0
S43	0	0	0	0	0	0	0	0	0	0	0	0	0	0
S44	0	0	0	0	0	0	0	0	0	0	0	1	1	1
S45	1	1	1	1	1	1	1	1	1	1	1	1	1	1
S46	1	1	1	1	1	1	1	1	1	1	1	1	0	0
S47	0	0	0	0	0	0	0	0	0	0	0	0	0	0
S48	0	0	0	0	0	0	0	0	0	0	0	0	1	1
S49	1	1	1	1	1	1	1	1	1	1	1	1	1	1
S50	1	1	1	1	1	1	1	1	1	1	1	1	1	0
S51	0	0	0	0	0	0	0	0	0	0	0	0	0	0
S52	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Table 3: Switching states and terminal voltages of twenty seven level CHBMLI with repeating sequence at negative side of segments

V_O	0	-vs	-2vs	-3vs	-4vs	-5vs	-6vs	-7vs	-8vs	-9vs	-10vs	-11vs	-12vs	-13vs
S1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
S2	1	1	1	1	1	1	1	1	1	1	1	1	1	1
S3	0	1	1	1	1	1	1	1	1	1	1	1	1	1
S4	0	0	0	0	0	0	0	0	0	0	0	0	0	0
S5	1	1	0	0	0	0	0	0	0	0	0	0	0	0
S6	1	1	1	1	1	1	1	1	1	1	1	1	1	1
S7	0	0	1	1	1	1	1	1	1	1	1	1	1	1
S8	0	0	0	0	0	0	0	0	0	0	0	0	0	0
S9	1	1	1	0	0	0	0	0	0	0	0	0	0	0
S10	1	1	1	1	1	1	1	1	1	1	1	1	1	1
S11	0	0	0	1	1	1	1	1	1	1	1	1	1	1
S12	0	0	0	0	0	0	0	0	0	0	0	0	0	0
S13	1	1	1	1	0	0	0	0	0	0	0	0	0	0
S14	1	1	1	1	1	1	1	1	1	1	1	1	1	1
S15	0	0	0	0	1	1	1	1	1	1	1	1	1	1
S16	0	0	0	0	0	0	0	0	0	0	0	0	0	0
S17	1	1	1	1	1	0	0	0	0	0	0	0	0	0
S18	1	1	1	1	1	1	1	1	1	1	1	1	1	1
S19	0	0	0	0	0	1	1	1	1	1	1	1	1	1
S20	0	0	0	0	0	0	0	0	0	0	0	0	0	0
S21	1	1	1	1	1	1	0	0	0	0	0	0	0	0
S22	1	1	1	1	1	1	1	1	1	1	1	1	1	1
S23	0	0	0	0	0	0	1	1	1	1	1	1	1	1
S24	0	0	0	0	0	0	0	0	0	0	0	0	0	0
S25	1	1	1	1	1	1	1	0	0	0	0	0	0	0
S26	1	1	1	1	1	1	1	1	1	1	1	1	1	1
S27	0	0	0	0	0	0	0	1	1	1	1	1	1	1
S28	0	0	0	0	0	0	0	0	0	0	0	0	0	0
S29	1	1	1	1	1	1	1	1	0	0	0	0	0	0
S30	1	1	1	1	1	1	1	1	1	1	1	1	1	1
S31	0	0	0	0	0	0	0	0	1	1	1	1	1	1
S32	0	0	0	0	0	0	0	0	0	0	0	0	0	0
S33	1	1	1	1	1	1	1	1	1	0	0	0	0	0
S34	1	1	1	1	1	1	1	1	1	1	1	1	1	1
S35	0	0	0	0	0	0	0	0	0	1	1	1	1	1
S36	0	0	0	0	0	0	0	0	0	0	0	0	0	0
S37	1	1	1	1	1	1	1	1	1	1	0	0	0	0
S38	1	1	1	1	1	1	1	1	1	1	1	1	1	1
S39	0	0	0	0	0	0	0	0	0	0	1	1	1	1
S40	0	0	0	0	0	0	0	0	0	0	0	0	0	0
S41	1	1	1	1	1	1	1	1	1	1	1	0	0	0
S42	1	1	1	1	1	1	1	1	1	1	1	1	1	1
S43	0	0	0	0	0	0	0	0	0	0	0	1	1	1
S44	0	0	0	0	0	0	0	0	0	0	0	0	0	0
S45	1	1	1	1	1	1	1	1	1	1	1	1	0	0
S46	1	1	1	1	1	1	1	1	1	1	1	1	1	1
S47	0	0	0	0	0	0	0	0	0	0	0	0	1	1
S48	0	0	0	0	0	0	0	0	0	0	0	0	0	0
S49	1	1	1	1	1	1	1	1	1	1	1	1	1	0
S50	1	1	1	1	1	1	1	1	1	1	1	1	1	1
S51	0	0	0	0	0	0	0	0	0	0	0	0	0	1
S52	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The above Table 2 and Table 3 show the switching combinations that generate the required Twenty Seven level output signals. The corresponding mode of operations of the cascaded H bridge multilevel inverter stages are described as follows.

a) Zero Output voltage (0Vs): Active switches S1,S2,S5,S6,S9,S10,S13,S14,S17,S18,S21,S22,S25,S26,S29,S30,S33,S34,S37,S38,S41,S42,S45,S46,S49,S50 are kept in ON and inverter output voltage is 0Vs.

b) Positive output voltage (+Vs): Active switches S1,S4,S5,S6,S9,S10,S13,S14,S17,S18,S21,S22,S25,S26,S29,S30,S33,S34,S37,S38,S41,S42,S45,S46,S49,S50 are kept in ON and inverter output voltage is Vs.

c) Positive output voltage (+2Vs): Active switches S1,S4,S5,S8,S9,S10,S13,S14,S17,S18,S21,S22,S25,S26,S29,S30,S33,S34,S37,S38,S41,S42,S45,S46,S49,S50 are kept in ON and inverter output voltage is 2Vs.

d) Positive output voltage (+3Vs): Active switches S1,S4,S5,S8,S9,S12,S13,S14,S17,S18,S21,S22,S25,S26,S29,S30,S33,S34,S37,S38,S41,S42,S45,S46,S49,S50 are kept in ON and inverter output voltage is 3Vs.

e) Positive output voltage (+4Vs): Active switches S1,S4,S5,S8,S9,S12,S13,S16,S17,S18,S21,S22,S25,S26,S29,S30,S33,S34,S37,S38,S41,S42,S45,S46,S49,S50 are kept in ON and inverter output voltage is 4Vs.

f) Positive output voltage (+5Vs): Active switches S1,S4,S5,S8,S9,S12,S13,S16,S17,S20,S21,S22,S25,S26,S29,S30,S33,S34,S37,S38,S41,S42,S45,S46,S49,S50 are kept in ON and inverter output voltage is 5Vs.

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g) Positive output voltage (+6Vs): Active switches S1,S4,S5,S8,S9,S12,S13,S16,S17,S20,S21,S24,S25,S26,S29,S30,S33,S34,S37,S38,S41,S42,S45,S46,S49,S50 are kept in ON and inverter output voltage is 6Vs.

h) Positive output voltage (+7Vs): Active switches S1,S4,S5,S8,S9,S12,S13,S16,S17,S20,S21,S24,S25,S28,S29,S30,S33,S34,S37,S38,S41,S42,S45,S46,S49,S50 are kept in ON and inverter output voltage is 7Vs.

i) Positive output voltage (+8Vs): Active switches S1,S4,S5,S8,S9,S12,S13,S16,S17,S20,S21,S24,S25,S28,S29,S32,S33,S34,S37,S38,S41,S42,S45,S46,S49,S50 are kept in ON and inverter output voltage is 8Vs.

j) Positive output voltage (+9Vs): Active switches S1,S4,S5,S8,S9,S12,S13,S16,S17,S20,S21,S24,S25,S28,S29,S32,S33,S36,S37,S38,S41,S42,S45,S46,S49,S50 are kept in ON and inverter output voltage is 9Vs.

k) Positive output voltage (+10Vs): Active switches S1,S4,S5,S8,S9,S12,S13,S16,S17,S20,S21,S24,S25,S28,S29,S32,S33,S36,S37,S40,S41,S42,S45,S46,S49,S50 are kept in ON and inverter output voltage is 10Vs.

l) Positive output voltage (+11Vs): Active switches S1,S4,S5,S8,S9,S12,S13,S16,S17,S20,S21,S24,S25,S28,S29,S32,S33,S36,S37,S40,S41,S44,S45,S46,S49,S50 are kept in ON and inverter output voltage is 11Vs.

m) Positive output voltage (+12Vs): Active switches S1,S4,S5,S8,S9,S12,S13,S16,S17,S20,S21,S24,S25,S28,S29,S32,S33,S36,S37,S40,S41,S44,S45,S48,S49,S50 are kept in ON and inverter output voltage is 12Vs.

n) Maximum positive output voltage (+13Vs): Active switches S1,S4,S5,S8,S9,S12,S13,S16,S17,S20,S21,S24,S25,S28,S29,S32,S33,S36,S37,S40,S41,S44,S45,S48,S49,S52 are kept in ON and inverter output voltage is 13Vs.

o) Negative output voltage (-Vs): Active switches S2,S3,S5,S6,S9,S10,S13,S14,S17,S18,S21,S22,S25,S26,S29,S30,S33,S34,S37,S38,S41,S42,S45,S46,S49,S50 are kept in ON and inverter output voltage is -Vs.

p) Negative output voltage (-2Vs): Active switches S2,S3,S6,S7,S9,S10,S13,S14,S17,S18,S21,S22,S25,S26,S29,S30,S33,S34,S37,S38,S41,S42,S45,S46,S49,S50 are kept in ON and inverter output voltage is -2Vs.

q) Negative output voltage (-3Vs): Active switches S2,S3,S6,S7,S10,S11,S13,S14,S17,S18,S21,S22,S25,S26,S29,S30,S33,S34,S37,S38,S41,S42,S45,S46,S49,S50 are kept in ON and inverter output voltage is -3Vs.

r) Negative output voltage (-4Vs): Active switches S2,S3,S6,S7,S10,S11,S14,S15,S17,S18,S21,S22,S25,S26,S29,S30,S33,S34,S37,S38,S41,S42,S45,S46,S49,S50 are kept in ON and inverter output voltage is -4Vs.

s) Negative output voltage (-5Vs): Active switches S2,S3,S6,S7,S10,S11,S14,S15,S18,S19,S21,S22,S25,S26,S29,S30,S33,S34,S37,S38,S41,S42,S45,S46,S49,S50 are kept in ON and inverter output voltage is -5Vs.

t) Negative output voltage (-6Vs): Active switches S2,S3,S6,S7,S10,S11,S14,S15,S18,S19,S22,S23,S25,S26,S29,S30,S33,S34,S37,S38,S41,S42,S45,S46,S49,S50 are kept in ON and inverter output voltage is -6Vs.

u) Negative output voltage (-7Vs): Active switches S2,S3,S6,S7,S10,S11,S14,S15,S18,S19,S22,S23,S26,S27,S29,S30,S33,S34,S37,S38,S41,S42,S45,S46,S49,S50 are kept in ON and inverter output voltage is -7Vs.

v) Negative output voltage (-8Vs): Active switches S2,S3,S6,S7,S10,S11,S14,S15,S18,S19,S22,S23,S26,S27,S30,S31,S33,S34,S37,S38,S41,S42,S45,S46,S49,S50 are kept in ON and inverter output voltage is -8Vs.

w) Negative output voltage (-9Vs): Active switches S2,S3,S6,S7,S10,S11,S14,S15,S18,S19,S22,S23,S26,S27,S30,S31,S34,S35,S37,S38,S41,S42,S45,S46,S49,S50 are kept in ON and inverter output voltage is -9Vs.

x) Negative output voltage (-10Vs): Active switches S2,S3,S6,S7,S10,S11,S14,S15,S18,S19,S22,S23,S26,S27,S30,S31,S34,S35,S38,S39,S41,S42,S45,S46,S49,S50 are kept in ON and inverter output voltage is -10Vs.

y) Negative output voltage (-11Vs): Active switches S2,S3,S6,S7,S10,S11,S14,S15,S18,S19,S22,S23,S26,S27,S30,S31,S34,S35,S38,S39,S42,S43,S45,S46,S49,S50 are kept in ON and inverter output voltage is -11Vs.

z) Negative output voltage (-12Vs): Active switches S2,S3,S6,S7,S10,S11,S14,S15,S18,S19,S22,S23,S26,S27,S30,S31,S34,S35,S38,S39,S42,S43,S46,S47,S49,S50 are kept in ON and inverter output voltage is -12Vs.

aa) Maximum Negative output voltage (-13Vs): Active switches S2,S3,S6,S7,S10,S11,S14,S15,S18,S19,S22,S23,S26,S27,S30,S31,S34,S35,S38,S39,S42,S43,S46,S47,S50,S51 are kept in ON and inverter output voltage is -13Vs.

III. PROPOSED TWENTY SEVEN LEVEL CASCADED H-BRIDGE MULTI LEVEL INVERTER (CHBMLI) WITH POD METHOD

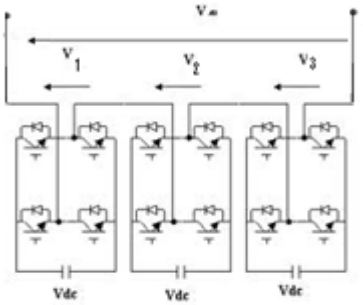

Fig.5: Twenty Seven level proposed CHBMLI

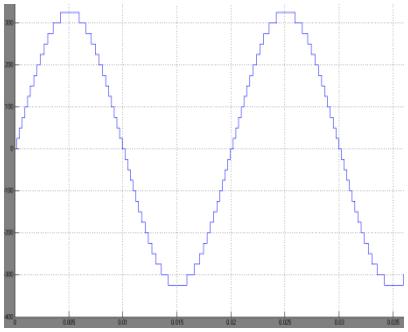

Fig.6. Output voltages of Twenty Seven level proposed CHBMLI

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Table 4: Switching states and terminal voltage of Twenty Seven level CHBMLI with phase opposition and disposition

Vo	Switches in proposed Cascaded H-Bridge Twenty Seven level Multi level inverter											
	S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12
+13Vs	1	1	0	0	1	1	0	0	1	1	0	0
+12Vs	1	0	1	0	1	1	0	0	1	1	0	0
+11Vs	0	0	1	1	1	1	0	0	1	1	0	0
+10Vs	1	1	0	0	1	0	1	0	1	1	0	0
+9Vs	1	0	1	0	1	0	1	0	1	1	0	0
+8Vs	0	0	1	1	1	0	1	0	1	1	0	0
+7Vs	1	1	0	0	0	0	1	1	1	1	0	0
+6Vs	1	0	1	0	0	0	1	1	1	1	0	0
+5Vs	0	0	1	1	0	0	1	1	1	1	0	0
+4Vs	1	1	0	0	1	1	0	0	1	0	1	0
+3Vs	1	0	1	0	1	1	0	0	1	0	1	0
+2Vs	0	0	1	1	1	1	0	0	1	0	1	0
+Vs	1	1	0	0	1	0	1	0	1	0	1	0
0	1	0	1	0	1	0	1	0	1	0	1	0
-Vs	1	1	0	0	1	0	1	0	1	0	1	0
-2Vs	0	0	1	1	1	1	0	0	1	0	1	0
-3Vs	1	0	1	0	1	1	0	0	1	0	1	0
-4Vs	1	1	0	0	1	1	0	0	1	0	1	0
-5Vs	0	0	1	1	0	0	1	1	1	1	0	0
-6Vs	1	0	1	0	0	0	1	1	1	1	0	0
-7Vs	1	1	0	0	0	0	1	1	1	1	0	0
-8Vs	0	0	1	1	1	0	1	0	1	1	0	0
-9Vs	1	0	1	0	1	0	1	0	1	1	0	0
-10Vs	1	1	0	0	1	0	1	0	1	1	0	0
-11Vs	0	0	1	1	1	1	0	0	1	1	0	0
-12Vs	1	0	1	0	1	1	0	0	1	1	0	0
-13Vs	1	1	0	0	1	1	0	0	1	1	0	0

The above Table 4 shows the switching combinations that generate the required Twenty Seven level output signals. The corresponding mode of operations of the cascaded H bridge multilevel inverter stages are described as follows.

a) Maximum output voltage (+13Vs & -13Vs): Active switches S1,S2,S5,S6,S9 and S10 kept in ON and inverter output voltage is 13Vs.

b) output voltage (+12Vs and -12Vs): Active switches S1,S3,S5,S6,S9 and S10 are kept ON and inverter output voltage is 12Vs.

c) output voltage (+11Vs and -11Vs): Active switches S3,S4,S5,S6,S9 and S10 are kept ON and inverter output voltage is 11 Vs.

d) output voltage (+10Vs and -10Vs): Active switches S1,S2,S5,S7,S9 and S10 are kept ON and inverter output voltage is 10Vs.

e) output voltage (+9Vs and -9Vs): Active switches S1,S3,S5,S7,S9 and S10 are kept ON and inverter output voltage is 9Vs.

f) output voltage (+8Vs and -8Vs): Active switches S3,S4,S5,S7,S9 and S10 are kept ON and inverter output voltage is 8.

g) output voltage (+7Vs and -7Vs): Active switches S1,S2,S7,S8,S9 and S10 are kept ON and inverter output voltage is 7Vs.

h) output voltage (+6Vs and -6Vs): Active switches S1,S3,S6,S7,S8,S9 and S10 are kept ON and inverter output voltage is 6Vs

i) output voltage (+5Vs and -5Vs): Active switches S3,S4,S7,S8,S9 and S10 are kept ON and inverter output voltage is 5Vs.

j) output voltage (+4Vs and -4Vs): Active switches S1,S2,S5,S6,S9 and S11 are kept ON and inverter output voltage is 4Vs.

k) output voltage (+3Vs and -3Vs): Active switches S1,S3,S5,S6,S9 and S11 are kept ON and inverter output voltage is -5Vs.

l) output voltage (+2Vs and -2Vs): Active switches S3,S4,S5,S6,S9 and S11 are kept ON and inverter output voltage is -5Vs.

m) output voltage (+Vs and -Vs): Active switches S1,S2,S5,S7,S9 and S11 are kept ON and inverter output voltage is Vs.

n) Zero output voltage: Active switches S1,S3,S5,S7,S9 and S11 are kept ON and inverter output voltage is Zero.

IV. SIMULATION RESULTS AND DISCUSSIONS

To validate the proposed topologies, numerical simulation studies have been carried out by using Matlab-Simulink. For the simulation studies the dc link voltage is taken as 350V. The parameters of the R & RL Loads used in this paper are R_l =51ohm, L_m=0.2mH. The simulation results of existing and proposed topologies are shown from Fig.7 – Fig.11.

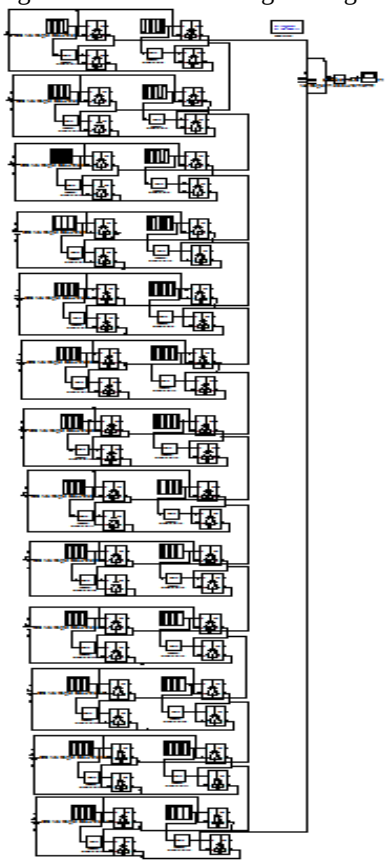

Fig.7. Repeating Sequence based Single Phase Twenty Seven level conventional CHBMLI With R & RL -Loads

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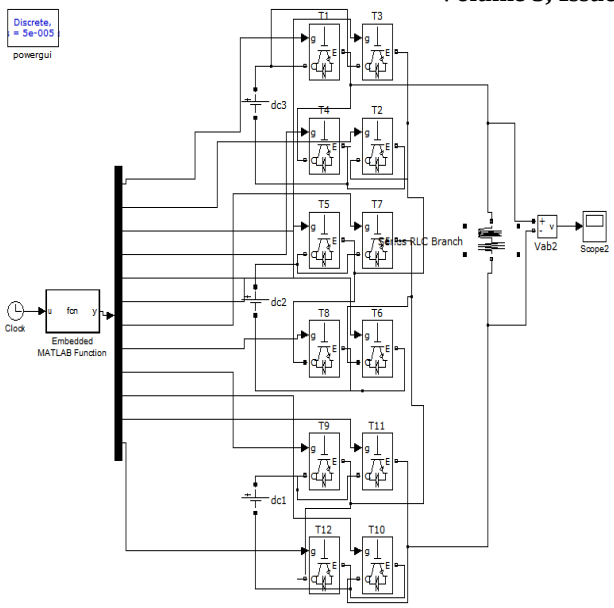

Fig.8. Phase opposition and disposition (POD) based Single Phase Twenty Seven level proposed CHBMLI With R & RL -Loads

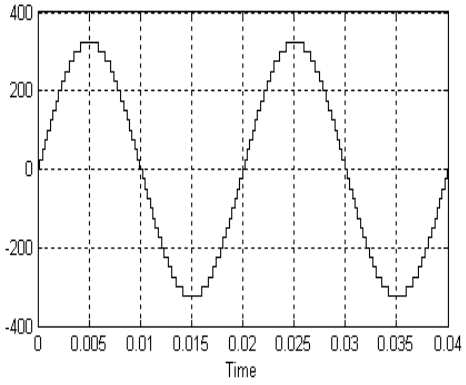

Fig. 9: Output Voltage waveforms of proposed Cascaded H-bridge with phase opposition & Disposition method With R & RL -Load

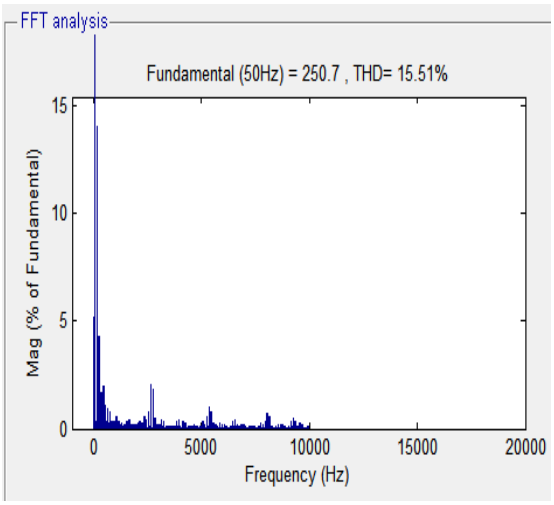

Fig.10: THD of Repeating Sequence based conventional Twenty seven levels CHBMLI With R & RL -Loads

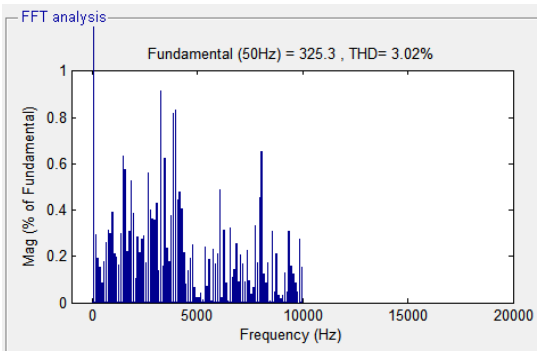

Fig.11: THD of Phase Opposition and Disposition based proposed Twenty seven level CHBMLI With R & RL –Loads

V. CONCLUSION

In this paper, the proposed POD based cascaded H- bridge multi level inverter topology offers strong advantages such as improved output waveforms, lower THD and lower electromagnetic interference. Here the performance of an asymmetrical configuration of Twenty Seven-level inverter (TSLI) based Cascaded H-Bridge Multi Level topology with R & RL loads is analyzed and compared with conventional CHBMLI with repeating sequence as switching technique. The performance factors are analyzed with the usage of minimum number of switches so that switching losses can be reduced effectively with proposed cascaded H-bridge multi level approach. From the THD patterns, it is observed that the magnitude of the THD is drastically reduced in POD modulation based CHBMLI when compared to conventional repeating sequence based CHBMLI.

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AUTHORS PROFILE

Mrs. B. Anusha graduated from KIET, Korangi. She is presently Pursuing M.Tech in the Department of Electrical and Electronics Engineering, Pragati Engineering college, Surampalem, Peddapuram A.P., INDIA. Her research areas include Multi level inverters, Power electronic Drives.

Dr. K. Satyanarayana obtained M.Tech degree in Power Electronics from JNTU College of Engineering, Hyderabad and Ph.D. from J.N.T.U. College of Engineering, Kakinada. He is presently working as Professor and H.O.D. of the Department of Electrical and Electronics Engineering, Pragati Engineering College, Surampalem, Peddapuram, A.P., INDIA. He presented 30 research papers in various national and international journals and conferences. His research interests include Power Electronic Drives, PWM, Multi Level Inverters and Vector Control Techniques. He is a member in editorial board of four journals. He is a member and charted Engineer in Institution of Engineers (India), life member in Indian Society for Technical Education and member in Institute of Electrical and Electronics Engineers.

Ms Ch. V. V. Manga Lakshmi Obtained M.Tech degree in Power Electronics and Electrical Drives from Pragati Engineering College, Surampalem. She is presently working as Assistant Professor in Electrical and Electronics Engineering Department of Pragati Engineering College, Surampalem, Peddapuram, A.P., INDIA. She presented many research papers at various international journals. Her research areas include Power Electronic Drives, Multi level inverters and PWM techniques.