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Optimum Design of Charge Pump Circuits Using Genetic Algorithm

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Abstract*— Integrated charge pump circuits are power converter used to obtain a different d.c levels. The most important performance parameters that effect the operation of these circuits may include voltage gain, ripple voltage, conversion efficiency, power consumption, and the chip area required for fabrication. Improvement of these parameters requires a trade-off between the above variables. Genetic Algorithm (GA) is employed in this paper as an optimization procedure to obtain an optimum design that satisfies a specified requirement. The GA realization is performed to concentrate on power consumption and chip area required. The other performance parameters are bounded as constrained variables. The resultant parameter values satisfy the minimum requirement for the designed fitness function while maintaing the other performances in their acceptable values.

***Index Terms*—Integrated CP design; Dickson CP; capacitive sizing; Genetic Algorithm and switch bootstrapped technique.**

I. INTRODUCTION

Charge pumps (CPs) are power converters that convert a d.c power supply to higher or lower level voltages. Charge pumps transfer charge packets from the power supply to the output terminal using only capacitors and switches to generate the required voltage level, this configuration allow integrated realization [1].

Integrated realization of charge pump circuits uses integrated capacitors as storage elements and transistors as transfer switches, where the drain and source terminals are the two switch terminals, and the gate terminal is used to control the switch state. Many integrated systems such as Flash memories, DRAMs, OTPs, RS-232 transceivers, and driver circuits require multiple supply voltage levels for their functional blocks and therefore charge pumps are needed [2].

The most important parameters that effect on performance of a CP is the number of stages, the required silicon area occupation and power consumption. Moreover, in the design of charge pumps with purely capacitive load, also the rise time and the charge consumption during the rise time are significant. However, it is worth noting that even if the clock frequency may appear as a design parameter, it is usually fixed at the value of the clock frequency of the host system [3].

Among many design approaches for charge pump, the switched-capacitor circuit such as Dickson charge pump is very popular, because it can be implemented on the same host system chip. The voltage gain (A_V) of Dickson charge pump is proportional to the number of stages (N) in the pump [4].

This work presents an optimization method that based on the use of Genetic Algorithm that deals conversion efficiency, voltage gain, load current as well as the silicon area and capacitor sizing of integrated CP. The aim of using GA is to minimize the total silicon area and power consumption while reserving the desired performances and specifications.

II. CHARGE PUMP CIRCUITS

Dickson Charge pump shown in Fig. (1) Comprises charge transfer diodes and charge pumping capacitors. Non-overlapping clock pulses is required to control the charge and discharge processes on the pumping capacitors. The circuit pumps charge from the power supply to the output terminal stage by stage to increase the output voltage V_o. The diodes are realized using NMOS transistors (Pass transistors). However, these diodes suffer from voltage loss because of the threshold voltage and body effect. The efficiency of the single Dickson CP is very low, especially at low input voltage. The double CP is conceived to reduce the output ripple by using the same total CP capacitance (C), as depicted in Fig. (2), each half part of clock pulse, which has a total capacitance C/2, feed the load in a different half period [3]. Hence, the charge pumped at the output is divided into two equal parts, each for half period of clock pulse. The output voltage is the same as the single Dickson CP, but the ripple is half as given [5]:

$$V_r = \frac{I_o}{2 * f * C_L} \quad (1)$$

Where V_r is the output ripple voltage, I_o is the loading current, C_L is the loading capacitance, and f is the frequency of clock pulse.

In the bootstrapped Dickson CP is shown in Fig. (3), the effect of switch voltage drop, varying on resistance, and low conduction are reduced by using four non-overlapping clock phases (F_1, F_2, FB_1 and FB_2) , which also prevent short-circuit currents from nodes at higher voltages to nodes at lower voltages. This configuration needs the generation of four appropriate clock phases and MOS switches able to withstand high voltages,this circuit involves sizing the boosting capacitor (C_b) adequately to bootstrap the gate of the pass transistors with the required overdrive voltage. The boosted voltage on the gate of the pass transistor is reduced because loading capacitance (C_L). The capacitors (C_b) must be able to supply sufficient voltage swing to the gate of the pass transistor and other parasitic capacitances. The boosted voltage can be given as [6]:

$$V_{dd} = 1 + \left(V_{DD} * \frac{C_b}{C_b + C_L}\right) \quad (2)$$

The bootstrapped double CP is shown in Fig. (4) is used to improve performance such as output voltage ripple

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reduction to half and increases efficiency and output voltages[3].

III. GENETIC ALGORITHM APPLICATION

Genetic Algorithm is a search technique based on the mechanics of natural selection used in computing to find true or approximate solutions to optimization and search problems. The simple GA begins with the creation of an initial random population of individualswith values that are chosen for the circuit variables, each of which represents a candidate solution to a given optimization problem. Genetic Algorithm is realized to obtain the optimum parameter values such as dimensions of the transistors, pumping capacitance, output voltage and loading currents. This is applied for the design and realization of conventional and bootstrapped charge pump circuits, single and double Dickson CP [7].

The first step in the GA process is to determine the topology of the design; the initial tasks of the minimization processes are the determining of search variables, specifications, and constraints in an appropriate manner. The variables are designed to be the widths of pass transistors (w), loading current (I_O), output voltage (V_O) and rising time (tr) of the response. It is required to satisfy the given desired specifications and constraints such as pumping capacitance (C), voltage gain (A_V), efficiency (η), current consumption (I_{DD}), charge consumption (Q_{TotN}), output ripple (V_r), output power (P_O) and minimum power consumption (P_{dsip}), total silicon area (A_{TotN}). The genetic algorithm process was realized as MATLAB program [3].

Two approaches can be used to represent each variable, real and binary representation methods are possible. In this work binary form that contains different binary code for each variable is individually chosen. Binary vector is designed as a chromosome to represent real values of the variables (I_O, w_1, V_O, V_O(tr), and tr). The length of the genes (each part of chromosome) depends on the required precision, which in this algorithm is three places after the decimal point [7]. The total length of designed chromosome found to be 75 bits. Using population size of 100, the total number of bit in population is 100 x 75 (randomly produced).

IV. FITNESS FUNCTION FORMULATION

The fitness function is formulated to include the specified variables in single chromosome. The fitness ofeach chromosome in the current population is then evaluated and tested. In general, the fitness functions can be expressed in single or multi-objective functions. Generally fitness function is defined as[8]:

$$Fitness(x) = \sum_{i=1}^{m} w_i \cdot Fit_i(x) \quad (3)$$

Where, w_i is the weight coefficient of every sub-objective, $Fit_i(x)$ is the fitness of every performance objective, $Fitness(x)$ is the overall fitness, and m is the number of the performance objective.The main objective function of the CPs under studied is constrained on power consumption and total chip area required for fabrication [9].

$$F_1 = \frac{1}{A_T} \quad (4)$$

$$F_2 = \frac{1}{P} \quad (5)$$

Where A_T is the total area in (μm^2), P is the total power consumption in (mW). The total area (A_T) can be given as:

$$A_T = \sum_{i=1}^{K} w_i \,.\, L_i + A_C \quad (6)$$

Where w_i and L_i are device dimensions, $K$is the number of transistors, and $A_C = \frac{C_{ox}}{C}$ is the area required to fabricate pumping capacitance for CP circuits.
The power consumption may be expressed as [3]:

$$P_{disp} = P = V_{DD} * I_{DD} \quad (7)$$

Where V_{DD} is the positive power supply voltage and I_{DD} is the current flow. Multi performance objectives can be included in single fitness function with proper choice of weight function to include total silicon area (A_T) and power consumption (P_{disp}) minimization as follows:

$$F = \frac{1}{A_T \times W_1 + P \times W_2} \quad (8)$$

Where W_1 and W_2 are the weighting factors.

According to the proposed GA realization shown in Fig. (5), evaluation of the fitness function for the current population (Pop_Size=100) is performed, and new population is generated if the requirements and constraints are found to be not satisfied. The new population is generated using probability distribution (Pc=0.6) based on fitness values, the selection process is based on spinning the roulette wheel population size times, each time it selects a single chromosome for a new population. The next operator is the recombination operator, a single point crossover applied to the individuals in the new population. One of the parameters of a genetic system is the probability of crossover Pc (probability rate). This probability gives the expected number (Pc x population size) of chromosomes which undergo to the crossover operation.The next operator, mutation, is performed on a bit-by-bit basis. Another parameter of the genetic system; probability of mutation Pm, the expected number of mutated bits is (Pm x m x population size), where m is the length of chromosome. Where (m=75, Pm=0.04, and Pop_Size=100). The number of mutated bits has been expected to be 317 bits mutations per generation. GA needs a halt condition to end the generations process. Among many stopping criteria [9], this work end the process if a specified number of generations is exceeded and the desired number of specifications is not

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reached, the algorithm stopped or when the fitness function evaluation is satisfied.

V. PERFORMANCES EVALUATION

The minimization of chip area and power consumption using GA effects other performances of CP circuits. The design equations forconventional and bootstrapped Dickson CP configurations that govern the performances can be derived, under the assumption that all the transistors in the circuits must be kept in the saturation region. These specifications may include output voltages, conversion efficiency, pumping capacitance, output ripple voltage, output power and current, charge consumption, and current consumption. The output voltage of the CP is given as [3]:

$$V_O = (1+N)\,V_{DD} - \frac{N I_O}{f * C} \tag{9}$$

Where N is the number of stages for CP circuits and $C$is the pumping capacitance. The current and charge consumption can be employed by equations with $\alpha = 0.1$. The number of stages in this work is determined to be four stages [3]

$$I_{DD} = \left[(1+N) + \alpha \frac{N^2}{(1+N)V_{DD} - V_O}.V_{DD}\right].I_O \tag{10}$$

$$Q_{TotN} = \left[(1+N)v_x + \alpha N^2 ln\frac{N}{1+N-v_x}\right]\left(\frac{C_T}{3} + C_L\right)V_{DD} \tag{11}$$

Where α is the parasitic factor and $v_x = \frac{V_O(tr)}{V_{DD}}$.

The pumping capacitance can be expressed as [3]:

$$C = \left[\frac{N}{(1+N)\,V_{DD} - V_O}.\,V_{DD}\right].\frac{I_O}{f} \tag{12}$$

The conversion efficiency of CP circuits is explained by follows as:

$$\eta(\%) = \frac{P_O}{P_{in}} = \frac{V_O * I_O}{I_{DD} * V_{DD}} \tag{13}$$

VI. GA RESULTS AND COMPARISON

The GA routine is used in this work to concentrate on minimization of power consumption and minimization of required chip area. The other performances that include voltage gain, pumping capacitance, efficiency, current and charge consumptions, ripple output voltage, and output power are used as constraints. The bound constraints for the selected variables are presented in Table (1). The GA resulted for these variables gives a significant improvement for the desired fitness variables compared with analytical counterpart as shown in Table (2). It can be seen from the above tables that GA results a significant improvement in chip area required and power consumption compared with the existing analytical approaches. However the other performances that selected as constraintsare slightly divert but their values are still in its bound conditions. Table (3) shows these performances for different load current. It is clear from this table that as I_o increases the pumping capacitance (C) increases since this capacitor is directly proportional to load current (I_o) [3].

VII. SIMULATION RESULTS

To certify the operation of CP circuits under the GA resultant parameter values. Orcad PSPICE is used to simulate the CP circuits under studied setting I_O = 600µA. The transient responses of these designs is shown in Fig. (6). It can be seen from this figure the optimum design parameters resulted from GA satisfy the desired requirement (output voltage, ripple output, rising time and efficiency). All CP circuits are designed and simulated under same conditions such as include stage capacitance, supply voltage, clock frequency, and identical device dimensions [9].

The output ripple voltages of these CP circuits are proportional to loading current, when increasing the current, the ripple outputs will be increase, the simulated of this relationship is shown in Fig. (7). The simulated output voltages of the CP designs with respected for changing in loading current is shown in Fig. (8). It can be seen from this figure the bootstrapped double CP has output voltages higher than from conventional single and double CP. Fig. (9) presents the output power for conventional and bootstrapped of single and double CP versus loading current with a pumping capacitance of 66.6pf and f=10MHz [5].

Fig. (10) Shows the simulated results of CP circuits with only capacitive load (C_L=200pf) and loading current (I_O=600µA) under different power supply voltages. The output voltages increases with increase power supply voltages. Also the four CP circuits are designed in the different input clock frequencies, the output voltages of these circuits are increased when the input clock signal frequencies is increased as shown in Fig. (11). However, the proposed charge pump (bootstrapped double CP) has higher output voltages under the same supply voltages and output current[3].

In the bootstrapped double charge pump give a higher output voltage under the same pumping capacitor, stage number (N=4), capacitive load, supply voltage, and same clock frequency, it indicates that the proposed CP circuit has better pumping efficiency than the single and double CP. The simulated power conversion efficiencies for the four stage charge pump circuits as functions of loading current, input supply voltages and input clock signal frequencies are shown in Figures 12, 13 and 14 respectively. The simulated maximum power efficiency of bootstrapped double CP is about 88.9% at f=10MHz and V_{DD}=1.8 V compared with the existing results in [3] as explained in tables 1 and 2.

VIII. CONCLUSIONS

This paper was concerned with the design and simulation of integrated charge pump circuits. An optimization procedures that based on the use of GA were applied to

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improve the circuit performances. A minimization of power consumption and total chip area required for fabrication were obtained compared with the existing results from analytical method. Simulation for different CP topologies using the resultant parameter values from GA showed the satisfaction between the specified requirement and GA results.As future extension of this work may include the use of multi-objective function that concentrate on other performances like pumping capacitance, number of stages, and efficiency.

REFERENCES

[1] G. Palumbo, D. Pappalardo, and M. Gaibotti, "Charge Pump Circuits: Power Consumption Optimization", IEEE Trans. Circuits Syst. I, vol. 49, no. 11, pp. 1535–1542, Nov. 2002.

[2] S. L.-K. Chang and C.-H. Hu, "High Efficiency MOS Charge Pumps Based On Exponential-Gain Structure With Pumping Gain Increase Circuits", IEEE Trans. Power Electronics, vol. 21, no. 3, pp. 826 –831, May 2006.

[3] G. Palumbo and D. Pappalardo, "Charge Pump Circuits: An Overview On Design Strategies And Topologies", IEEE Circuits Syst. Mag., vol. 10, no. 1, pp. 31 –45, 2010.

[4] Aamna Anil and Ravi Kumar Sharma, "A High Efficiency Charge Pump For Low Voltage Devices", International Journal of VLSI design & Communication Systems (VLSICS) Vol.3, No.3, Lovely Professional University, Jalandhar, Punjab, India, June 2012.

[5] Robert J. and PrimitModi , "A Charge Pump Architecture With High Power Efficiency And Low Output Ripple Noise In 0.5 MmCMOS Process Technology", M.Sc. Thesis, Electrical and Microelectronics Engineering, Rochester, New York, July, 2012.

[6] Stefano Gregori and YounisAllasasmeh, "Switch Bootstrapping Technique For Voltage Doublers And Double Charge Pumps", in Proc. IEEE Int. Symp. Circuits Syst. (ISCAS), 2011, pp. 494-497.

[7] Z. Michalewica, "Genetic Algorithms + Data Structures = Evolution Programs", Springer-Verlag Berlin Heidelberg, University of North Carolina, 1996.

[8] M. Melanie, "An Introduction To Genetic Algorithms", MIT press, 1998.

[9] R. L. Haupt and S. E. Haupt, "Practical Genetic Algorithms", John Wiley and Sons. Second edition, 2004.

Table 1: GA results for the designed variables

Variables	Lower bound	Upper bound	GA result	Analytical
Io (µA)	100	1100	600	600
w1(µm)	0.18	18	14.3	18
Vo (V)	4.2	9	5.55	7.2
Vo(tr) (V)	0	5.2	2.74	5.2
Tr (µs)	0	10	6	10

Table 2: GA results for integrated CP circuits designs with I_o=600µA and CL=200 pf

Specification	Type	Desired values	GA results	Analytical
Area (μm^2)	Fitness Function	Fitness (Min)	1.15	2.3
Power consumption(mW)	Fitness Function	Fitness (Min)	5.23	7.15
Voltage gain Av (dB)	Constraints	≤ 33	32.18	32.18
Pumping capacitance C (pf)	Constraints	≤ 120	66.67	65.8
Efficiency η (%)	Constraints	≥ 55	63.2 %	44.8%
I_{DD} (mW)	Constraints	≤ 38	3.48	4.25
Q_{TotN} (nC)	Constraints	≤ 6	2.85	12.2
Ripple Voltage Vr (Volt)	Constraints	≤ 0.55	0.3	0.3
Output power P_O (mW)	Constraints	≤ 8	3.3	4.3

Table 3: Performance specification for change Io from 0.1mA to 1.1mA

Io (µA)	C (pf)	Vr (V)	Av (dB)	$w_1..w_5$ (µm)	I_{DD} (mA)	Po (mW)	Pin (mW)
365	39.6	0.17	32.2	14.8	2.5	2.71	4.5
600	66.6	0.3	32.2	14.3	3.48	3.3	5.23
700	77.8	0.35	32.2	2.688	4.1	3.92	6.2
811	90.1	0.41	32.2	13.3	9.4	7.2	12.2

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Volume 5, Issue 5, November 2015

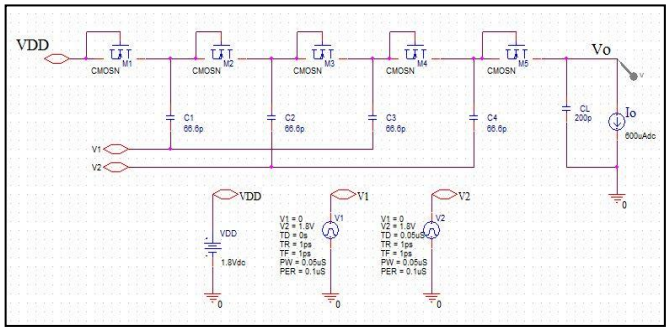

Fig (1): Conventional single Dickson CP circuit

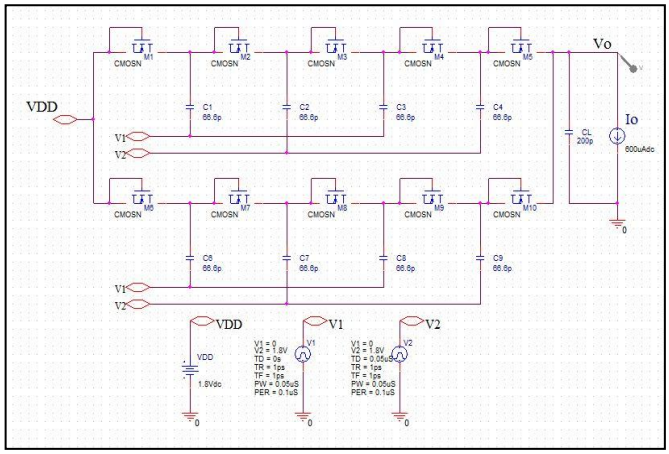

Fig (2): Conventional double Dickson CP circuit

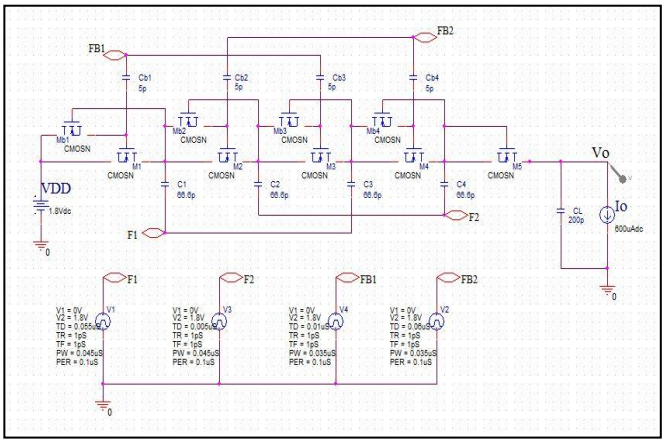

Fig (3): Bootstrapped single Dickson CP circuit

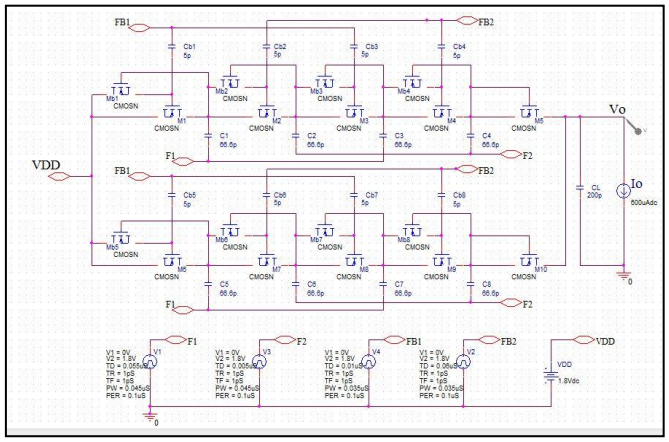

Fig (4): Bootstrapped double Dickson CP circuit

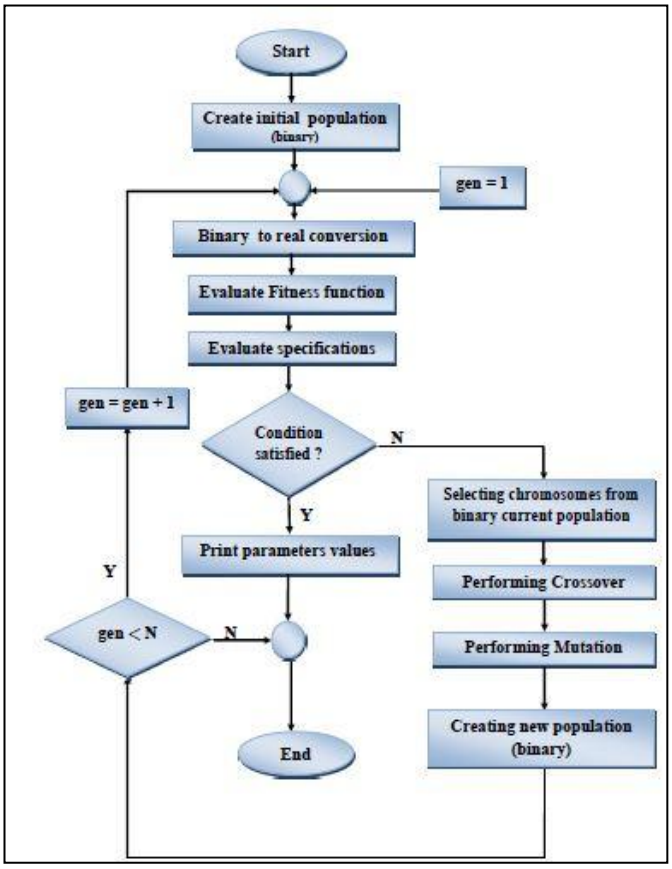

Fig (5): Flow chart for GA process

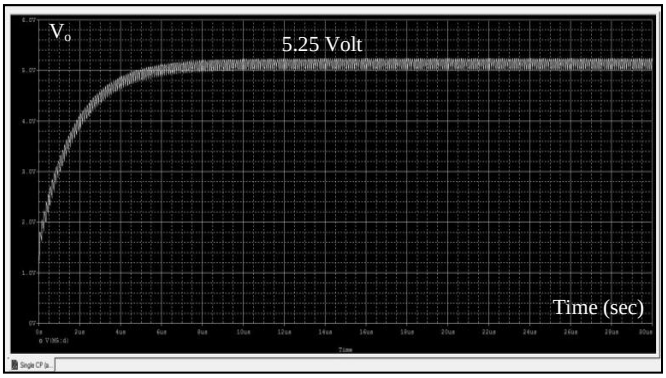

Fig (6): Transient response of the Dickson CP circuits

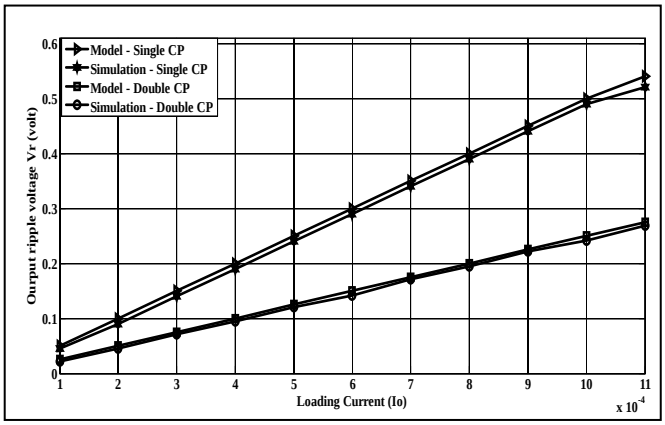

Fig (7): Model and simulation of loading current versus output ripple voltages for single Dickson charge pump and double CP

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International Journal of Engineering and Innovative Technology (IJEIT)
Volume 5, Issue 5, November 2015

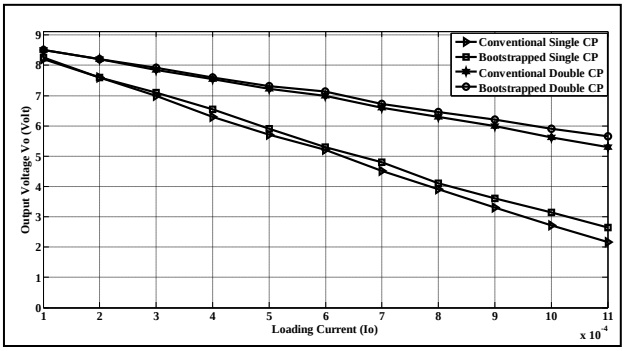

Fig (8): Simulated output voltages versus loading current for conventional and bootstrapped of single and doubleCP with $N = 4,\ f = 10MHz,\ V_{DD} = 1.8\,V\ and\ C = 66.6pf$

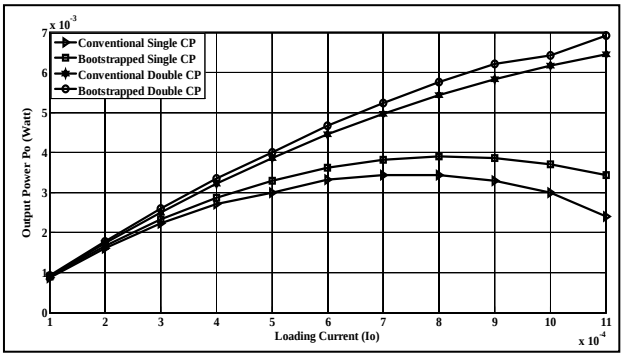

Fig (9): Output power variation with respect loading current for conventional and bootstrapped of single and double CP with $f = 10MHz,\ V_{DD} = 1.8\,V\ and\ C = 66.6pf$

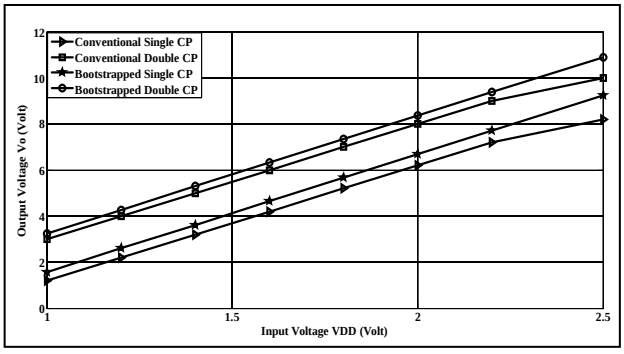

Fig (10): Simulated output with respect to change in the input voltage for conventional and bootstrapped of single and double CP with $f = 10MHz,\ Io = 600\mu A\ and\ C = 66.6pf$

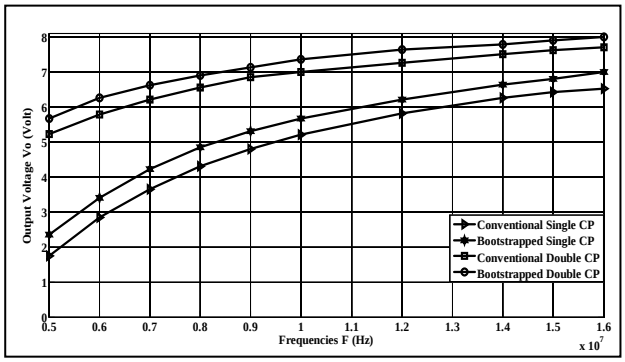

Fig (11): Simulated outputs variation versus input frequencies for conventional and bootstrapped of single and double CP with $Io = 600\mu A,\ V_{DD} = 1.8\,V\ and\ C = 66.6pf$

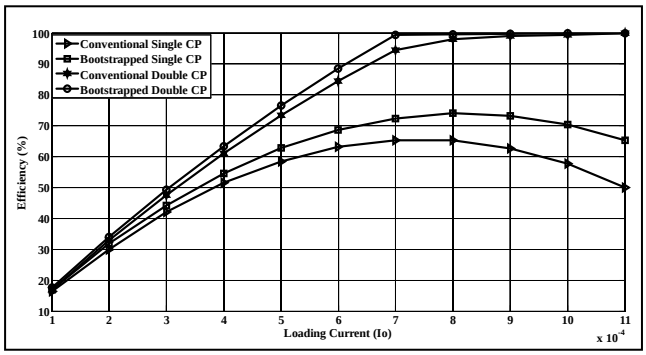

Fig (12): Simulated efficiency variation versus loading current for conventional and bootstrapped of single and double Dickson CP with $f = 10MHz,\ V_{DD} = 1.8\,V\ and\ C = 66.6pf$

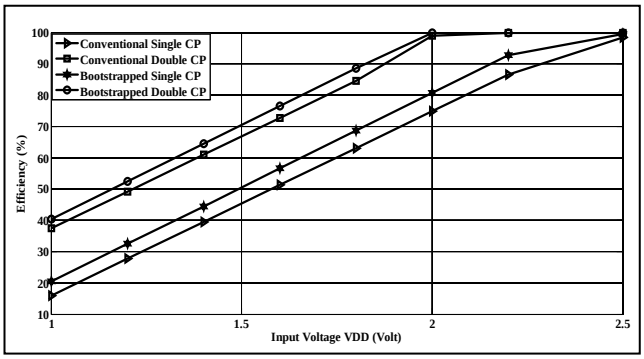

Fig (13): Simulated efficiency variation versus input voltages for conventional and bootstrapped of single and double Dickson charge pump with $f = 10MHz,\ Io = 600\mu A\ and\ C = 66.6pf$

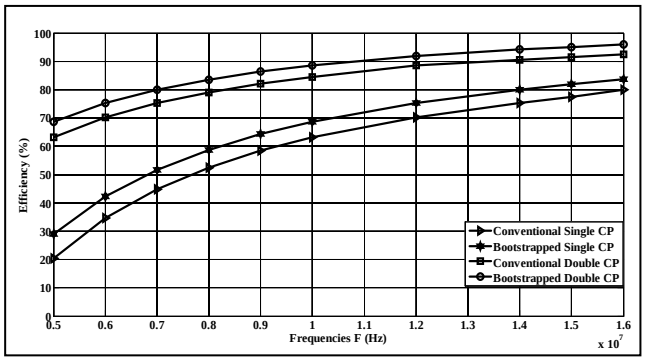

Fig (14): Simulated efficiency variation versus input frequencies for conventional and bootstrapped of single and double CP with $Io = 600\mu A,\ V_{DD} = 1.8\,V\ and\ C = 66.6pf$

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