ISSN: 2277-3754
ISO 9001:2008 Certified
International Journal of Engineering and Innovative Technology (IJEIT)
Volume 4, Issue 5, November 2014

A New Empirical I-V Model of CNTFETs for the Design of Electronic Circuits

Agostino Giorgio DEI – Politecnico di Bari

***Abstract*—In this letter it is proposed a fully empirical current-voltage (I-V) model of the Carbon Nanotube Field Effect Transistor (CNTFET) based on an empirical approach to overcome the drawbacks of the currently used models. The empirical approach in past has been successfully applied by the author to the characterization of GaAs MESFETs but has never been applied until now to the characterization of the CNTFET. The proposed model is very compact, fast and accurate, without any physical approximation, and then it is particularly suitable for the design of CNTFETs-based electronic circuits.**

Index Terms—**Carbon Nanotubes, Electronic circuits design, Field Effect Transistors, modeling, FETtoy.**

I. INTRODUCTION

The most recent efforts of the electronics technology are aimed at overcoming the challenges arising from the scaling of the silicon (Si) technology because the scaling trend still continues; anyway, bulk Metal Oxide Field Effect Transistors (MOSFETs) will soon reach their limiting size. Therefore, researchers are investigating more futurist materials and devices as carbon nanotubes (CNTs) and CNTFETs [1] to integrate and perhaps to replace, in the long run, the current silicon-based technology due to their exceptional properties. In fact, CNTs depending on the orientation in which graphene sheets are rolled (chirality) perform a metal-like behavior, able to carry very high current density (about 10 □ A/nm^2), or a semiconductor-like behavior, exhibiting near-ballistic, scattering-free, charge transport characteristics [2]. These features result in scattering-free, high speed CNTFETs and in considerable advantages over the nanoscale, MOSFETs best performances. However, the physical mechanisms governing the operation of CNTFETs are complex and difficult to model with mathematical equations at the same time accurate, compact and quickly running [3]. In fact, the development and execution of accurate physical models requires the numerical solution of the dispersion relation of the graphene, the non-equilibrium Green's function and the Schrodinger and Poisson equations (SP-solver). Then, accurate physical models are so complex, very time-consuming to perform calculations and therefore they are oriented to the analysis of devices but they are not so useful for the design of circuits. In order to obtain quite simple and compact physical models a number of approximations are needed resulting in lower accuracy especially for high drain-source voltages, i.e. V_{DS}>1V. In this letter, a new, very fast, simple and accurate model of CNTFETs is proposed, available for any applied voltage and for any diameter of the CNT, being the model based on an empirical approach. It is not required the measurement of S-parameters and of parasitic resistances. Such a model is suitable to fit I-V curves of the device either measured or calculated by other more complex models, with the aim to replace them for circuits design purposes, without losing accuracy. In fact, any software for circuits design needs analytical models of the devices (transistors) used to build the circuit. Simpler and more accurate are the models of the devices, and then faster and more accurate is the design of electronic circuits. The letter is so organized: in section II the proposed model is described; in section III the model is verified through the comparison of the modeled I-V characteristics of single-wall (SW) MOSFET-like CNTFETs with the same curves obtained by using the accurate numerical simulator FETtoy [4]; conclusions are in section IV.

II. MODEL DESCRIPTION

An empirical I-V model of an electronic device uses mathematical functions whose shape is similar to reference I-V curves to match, obtained by current-voltage measurements or by accurate numerical calculations [5]. Empirical parameters properly inserted into mathematical equations, enable modelled curves to match reference I-V curves as well as possible. To determine the value of these empirical parameters, it is required a numerical algorithm minimizing the absolute error between reference and modeled I-V values. This is the parameter extraction procedure. Then, an empirical model is much more suitable to fast convergence performance, computing time and accuracy than a physical model and does not require any approximation. On the other hand, it may be far from the intuition of the physical mechanisms governing the behavior of the device. Then, attention is generally required to determine the initial estimation of the empirical parameters to start the extraction routine. However, in the proposed model, considerations relevant to the electrical behavior of the device allow to perform the initial values estimation of the empirical parameters to run the extraction routine, thus resulting particularly easy and quick. Moreover, the CNTFETs I-V values are generally calculated as a function of internal voltages, i.e. considering the voltage drop due to the source and drain parasitic resistances. This is a serious limitation because these resistances depend on the bias conditions and a constant approximated value is generally used. This approximation does not persist in the new model by using the voltages directly applied at the device external terminals. Therefore, the model needs no calculation of parasitic resistances and there is not any approximation. Finally, the new model proves accurate for any geometrical feature of the CNTFET and in any bias condition.

The proposed I-V model equation is:

$$I_{DS} = [I_{DSS0} + G_1 V_G + K_2 {V_G}^2](\lambda_0 + \lambda_1 V_{DS})[\tanh(\alpha V_{DS})]^M \tag{1}$$

I_{DS} is the drain-source current, V_{GS} is the gate-source voltage, V_{DS} is the drain-source voltage.

Moreover, it holds:

$$V_G = V_{GS} - V_t \tag{2}$$

$$V_t = V_{th} + \gamma V_{DS} V_{GS} \tag{3}$$

Where I_{DSS0}, G_1, K_2, V_{th}, λ_0, λ_1, γ, α, M, are the empirical parameters of the model. Moreover, V_t is the threshold voltage of the device, being V_{th} the threshold voltage at zero bias The model equation (1) has a very simple explanation. In fact, the use of the hyperbolic tangent function is because this function follows typical I_{DS}-V_{DS} curves of field effect transistors (FETs) for low V_{DS} voltages, and then it is a very useful function to the aim of empirical modeling [5]. Then, parameters α and M allow the best fit between modeled and reference I_{DS}-V_{DS} curves for low V_{DS} values, i.e. in the so called “knee region” and in the “linear region” of the device characteristics (see fig. 1), here modifying the behavior of the hyperbolic tangent function. The parameter M does not depend on the V_{GS} voltage; on the contrary, the parameter α depends on the V_{GS} voltage as in (4):

$$\alpha = a_0 + a_1 V_{GS} + a_2 {V_{GS}}^2 + a_3 {V_{GS}}^3 \tag{4}$$

The term ($\lambda_0 + \lambda_1 V_{DS}$) models the drain control over I_{DS} in the saturation region, which is defined for “higher” V_{DS}, more precisely for $V_{DS} \geq V_{DSAT}$ where V_{DSAT} is the saturation drain-source voltage, i.e. that value of V_{DS} corresponding to the end of the knee region of I_{DS}-V_{DS} curves.

The term ($I_{DSS0} + G_1 V_G + K_2 V_G^2$) models the gate control over I_{DS}. In fact, it is a more general expression of the approximated FET trans-characteristic: $I_{DS} = I_{DSS}(1-V_{GS}/V_t)^2$

Equation (3) models the shift of the threshold voltage at zero bias V_{th}, due to a number of conduction phenomena happening in CNTFETs so difficult to model accurately with physical equations. The extraction procedure to calculate the values of the empirical parameters, searches for the best fit (i.e. the minimum error) between the reference and the modeled I_{DS}-V_{DS} curves. The initial estimation of the empirical parameters of the model, necessary to start the extraction routine, is facilitated by the meaning of the terms of the model that we have just explained. In fact, I_{DSS0}, K_2 and G_1 are estimated as the coefficients of the second-order polynomial interpolating the maximum saturation drain-source reference current (I_{DSS}) as a function of the voltage V_{GS}.

Initial values of λ_0, λ_1, and γ, should be set equal to zero due to the electrical behavior of an ideal CNTFET. In fact, in an ideal CNTFET, there is no shift in the threshold voltage (γ=0) and there is a full gate control over the current (i.e. there is no drain control over the current in the saturation region resulting $\lambda_0 = \lambda_1 = 0$). The initial value of α parameter can be easily estimated considering that the hyperbolic tangent function approaches to unity when its argument is large enough, i.e. when $\alpha V_{DS} \geq 6$. In this condition, the I_{DS} current of the CNTFET in the saturation region is almost constant. Therefore, in the saturation region it holds $\tanh(\alpha V_{DSAT}) \to 1$ i.e. $\alpha V_{DSAT} \geq 6$. Then, it is easy to estimate as initial values $\alpha = 6/V_{DSAT}$.

The initial value of M parameter can be easily estimated considering that it modifies the hyperbolic tangent shape especially in the knee region of I-V curves. Therefore, giving M = 1 as initial value of M to start the parameter extraction routine, is a useful choice.

Finally, the threshold voltage V_{th} can be initially estimated as a half of the band gap E_{bg} of the CNT acting as the channel of the CNTFET as [6]:

$$V_{th} \simeq \frac{E_{bg}}{2e} = \frac{aV_\pi}{eD_{CNT}} \simeq \frac{0.436}{D_{CNT}(nm)} \tag{5}$$

Where e is the electron charge, a ≈ 0.144 nm is the length of the carbon-carbon bond, $V_\pi \approx 3.033$eV is the energy of the π–π bond and D_{CNT} is the diameter of the CNT (channel).

The extraction routine which starts with these initial values of the empirical parameters results fairly quick, running in a few seconds, and unique.

III. RESULTS

The proposed model has been validated by comparisons with reference I_{DS}-V_{DS} curves obtained by the numerical model implemented in the FETtoy tool [4]. The calculations have been performed for a MOSFET-like CNTFET, having oxide thickness $t=1.5nm$, diameter $D_{CNT}=2nm$, threshold voltage $V_{th}=0.2V$, SiO2 as gate dielectric.

Fig. 1 shows the I_{DS}-V_{DS} curves for different values of V_{GS} and for V_{DS} up to 3V

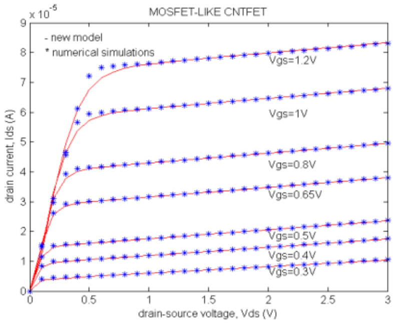

Fig. 1. I_{DS}-V_{DS} curves with different values of V_{GS}

The mean percentage error between the I_{DS} calculations performed by the FETtoy simulator and by the new model is about of 0.9%. In fig. 2 the drain current versus the gate voltage (I_{DS}-V_{GS}) curves are plotted for different values of V_{DS}. In table I there are the values of the empirical parameters calculated by the minimization routine. These values hold for fig. 1and 2. It is evident that the new model I_{DS} calculations for low and high voltages applied are closed to those by FETtoy simulator. The comparisons where performed also for I_{DS}-V_{DS} curves determined for different values of the CNT diameter which have significance effects on I_{DS} due to the energy gap of all sub bands are inversely proportional to the CNT diameter [1].

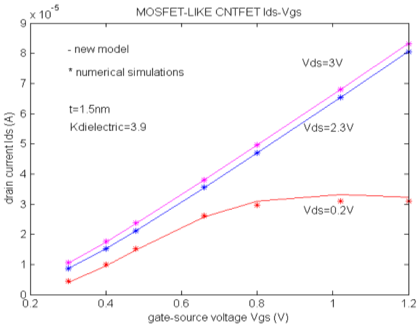

Fig. 2. I_{DS}-V_{GS} curves with different values of V_{DS}

Fig. 3 shows the I_{DS}-V_{DS} reference and modeled curves obtained for V_{GS} = 0.8V and for three different values of the CNT diameter: D_{CNT} = 1nm, 3nm and 5nm respectively. In table II there are the values of the empirical parameters. Also in this case the mean percentage error between current calculations performed by the FETtoy simulator and by the new model is less than 1%

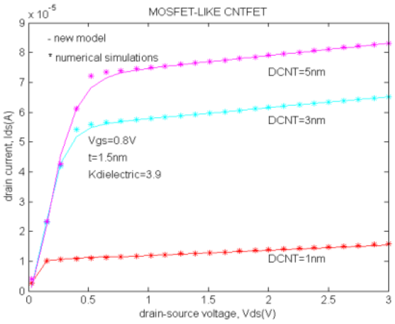

Fig. 3. I_{DS}-V_{DS} curves for different values of the diameter D_{CNT}

IV. CONCLUSIONS

In this letter a new, very fast and accurate empirical model of CNTFETs has been proposed. The model has been validated by comparisons with results obtained by the last release of the numerical simulator FETtoy. The percentage mean error is less than 1% for all I_{DS}-V_{DS} calculations performed for different values of V_{GS} and of the CNT diameter, as for low as for high bias voltages. The need for a procedure of extraction of the model parameters appears as the only drawback of the model but it is easily, quickly and accurately performed also because it is possible to easily perform an estimation of the model parameters to start the extraction routine very close to their final values. No S parameters and no parasitic resistances have to be determined. We can conclude that the fully empirical approach is very suitable for the design of analog and digital circuits based on CNTFETs and the new empirical model due to its accuracy and compactness can replace the more complex and time consuming SP-solver in the design of complex circuits.

Table I – Empirical parameters values for different values of the polarization gate-source voltage V_{GS}

V_{GS} (V)	I_{DSS0} (μA)	G_1 (e^{-2} S)	K_2 ($\mu A/V^2$)	λ_0 (e^{-6})	λ_1 (e^{-6} V^{-1})	α (V^{-1})	M	V_{th} (V)	γ (V^{-1})
0.3	1.9e^3	1.65	-63	3.72	2.26	18.59	1.62	0.24	-0.3
0.4	1.9e^3	1.65	-63	9.18	2.78	14.86	1.62	0.24	-0.3
0.5	1.9e^3	1.65	-63	14.60	3.02	12.40	1.62	0.24	-0.3
0.65	1.9e^3	1.65	-63	28.44	3.22	8.32	1.62	0.24	-0.3
0.8	1.9e^3	1.65	-63	39.80	3.27	6.27	1.62	0.24	-0.3
1	1.9e^3	1.65	-63	57.99	3.32	4.38	1.62	0.24	-0.3
1.2	1.9e^3	1.65	-63	73.07	3.35	3.48	1.62	0.24	-0.3

Table II – Empirical parameters values for different values of the diameter

V_{GS} =0.8 V	I_{DSS0} (μA)	G_1 (e^{-2} S)	K_2 ($\mu A/V^2$)	λ_0 (e^{-4})	λ_1 (e^{-5} V^{-1})	α	M	V_{th} (V)	γ (V^{-1})
d = 1nm	1	0	0	0.10	0.17	13.48	1.20	0.44	0
d = 3 nm	1	0	0	0.54	0.37	4.91	1.78	0.15	0
d = 5 nm	1	0	0	0.70	0.41	3.80	1.76	0.09	0

REFERENCES

[1] R. Chau, S. Datta, M. Doczy, B. Doyle, B. Jin, J. Kavalieros, A. Majumdar, M. Metz, and R. Radosavljevic, “Benchmarking nanotechnology for high-performance and low-power logic transistor applications”, IEEE Trans. Nanotechnol., vol. 4, no. 2, pp. 153-158, Mar 2005.

[2] A. Raychowdhury, A. Keshavarzy, J. Kurtin, V. De, and K. Roy, “Carbon Nanotube field-effect transistors for high-performance digital circuits – DC analysis and modeling

toward optimum transistor structure", IEEE Trans. Electron Devices, vol. 53, n. 11, pp. 2711-2717, Nov. 2006

[3] M. Claus, M. Haferlach, D. Gross, and M. Schroter, "Critical review of CNTFET compact models", in Proc. WCM, Int. NanoTech Meeting, pp. 770-775, June 2012

[4] A. Rahman, J. Guo, Md. Sayed Hasan, Y. Liu, A. Matsudaira, Shaikh S. Ahmed, S. Datta, and M. Lundstrom, (2014) "FETToy," On line https://nanohub.org/resources/fettoy . (DOI: 10.4231/D3RV0D12Z).

[5] A. Giorgio, V... M. N. Passaro, and A. G. Perri, "DC thermal modeling of GaAs MESFETs based on a semi empirical approach", International Journal of Electronics, vol. 88, no. 8, pp. 861-871, 2001

[6] M. Hossein Moaijeri, R. Faghih Mirzaee, A. Doostaregan, K. Navi, and O. Hashemipour, "A Universal method for designing low-power carbon nanotube FET-based multiple valued logic circuits", IET Comput. Digit. Tech., vol. 7, no. 4, pp. 167-181, 2013.

AUTHOR'S PROFILE

Agostino Giorgio was born in Bari, Italy, in 1969. He received the laurea degree cum laude in Electronic Engineering from the Polytechnic of Bari in April 1994. From 1994 he was with the Polytechnic of Bari where he held the position of Assistant Professor of Electronics. He is also the head of Digital Electronics Lab. His research activities are in the area of modeling of electronic devices, PBG-based devices, and digital electronics for telemedicine and home care applications. He is author of a number of papers and of 15 research and teaching books, also.