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Simulation and Comparision of Single Phase and Three Phase 7 level Multilevel inverter

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Abstract*— This paper present a asymmetrical cascaded 7 level multiinverter using fixed frequency carrier based pulse width modulation technique. The multilevel inverter is used to reduce harmonics. Here we are comparing single phase 7 levels and 3 phase seven level topology and thus reducing THD less than 5%. In asymmetrical cascaded single phase MLI by using only 2-H bridges with 8 switches we can get 7 level output voltage where as cascaded three phase MLI 7 level output voltage is obtained by using 6-H bridges with 24 switches.

***Index Terms*— Asymmetric CMLI, level shifted PWM, THD, PD POD, APOD, RL load**

I. INTRODUCTION

In recent years the Multi-Level Inverters are very popular for Industrial and powers system applications due to their advantages on two-level inverters i.e. High Power rating, Low Harmonics so they give the higher efficiency. The different topologies of Multi-Level Inverters are Neutral-point clamped (NPC) or Diode Clamped (DC) inverter, Flying capacitor inverter and Cascade inverter. As the level increases, NPC require more clamping diodes so the control of real power flow becomes very difficult. In flying capacitor inverter as the level increases, number of storage capacitors also increases hence they becomes bulky and costly; there are more switching losses in this topology. The cascaded multilevel inverters have more advantages than other topologies, because it does not require any balancing capacitors and diodes. Cascaded inverters need separate DC sources for each H-Bridge, so there is no voltage balancing problem but isolated DC sources are not readily available, this is the main drawback of this topology.

I1. ASYMMETRIC CASCADED MULTILEVEL INVERTER TOPOLOGY

Asymmetric multilevel have the same topology as symmetric multilevel inverters. They differ only in the rating of input dc voltages and control strategies. For many applications it is difficult to use separate dc sources and too many dc sources will require many long cables and could lead to voltage imbalance among the dc sources. To reduce the number of dc sources required for the cascaded H-bridge multilevel inverter, a scheme is proposed which uses lesser number of bridges. This scheme therefore provides the capability to produce higher voltages at higher speeds with low switching frequency which has inherent low switching losses and high converter efficiency. A seven-level asymmetric cascaded H bridge multilevel inverter has two H-bridges for each phase. The DC source for the first H-bridge (H1) is Vdc/2, while the DC source for the second bridge (H2) is Vdc. In asymmetrical single phase cascaded H- bridge multilevel inverter we are using two dc source,2 H-bridge,8 Switches, and in asymmetrical three phase cascaded H-bridge,we are using ,6 dc source,3 H-bridge,24 switches. Vdc1=210.6,Vdc2=105.3. . The switching states of asymmetrical seven level output voltage is given in the Table. 1.

switch	A	B	C	D	E	F	G	H
Vdc	1	0	1	0	1	0	0	1
2Vdc	0	1	1	0	0	1	0	1
3Vdc	1	0	1	0	0	1	0	1
0	0	0	0	0	0	0	0	0
-Vdc	0	1	1	0	1	0	1	0
-2Vdc	0	1	0	1	1	0	0	1
-3vdc	0	1	0	1	1	0	1	0

III. LEVEL SHIFTED PULSE WIDTH MODULATION

Modulation methods developed for multilevel inverters involve multilevel sinusoidal pulse width modulation, multilevel selective harmonic elimination and space-vector modulation. It is generally accepted that the performance of any inverter, with any switching strategy can be related to the harmonic contents of its output voltage. There are many control techniques reported for cascaded multilevel inverter. But the popularly used modulation method is the multicarrier level shifted PWM technique. Level shifted PWM technique is the generally used method in cascaded multilevel inverter as it gives a reduced THD. In this paper, fixed frequency PWM is proposed which uses the conventional sinusoidal reference signal and the carrier signals with variable frequency. To implement a m-level inverter, (m-1) carriers are used. There are six distinct carriers with fixed frequency and with the same magnitudes for the seven level multilevel inverter; the difference between the carriers is that they are all displaced by a set of DC offset. The frequency modulation index is given by mf = fc /fm

Where fc = carrier frequency

fm = modulating waveform frequency

Where as the amplitude modulation index is defined as the ratio of Vr/Vc

ma = Vm/Vcr(m-1) for $0 \leq ma \leq 1$

Where Vm = peak value of the modulating waveform\

Vcr = peak value of the carrier waveform

the switching frequency of the inverter using the Level-shifted modulation is equal to the carrier Frequency, that is,

fsw,inv = fcr

and the average device switching frequency is

fsw,dev = fcr / 2N

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The following figures shows the simulated waveforms for a seven-level inverter operating under the condition of fm = 50 Hz, and fcr = 2850 Hz. Although the carrier frequency of 2850 Hz seems high for high-power converters, the average device switching frequency is only 712 Hz. Figure 1,2 and 3 shows three schemes for the level-shifted multicarrier modulation:(a) phase disposition (PD), where all carriers are in phase; (b)alternative phase opposite disposition (APOD),where all carriers are alternatively in opposite disposition; and (c) phase opposite disposition (POD), where all carriers above the zero reference are in phase but in opposition with those below the zero reference.,

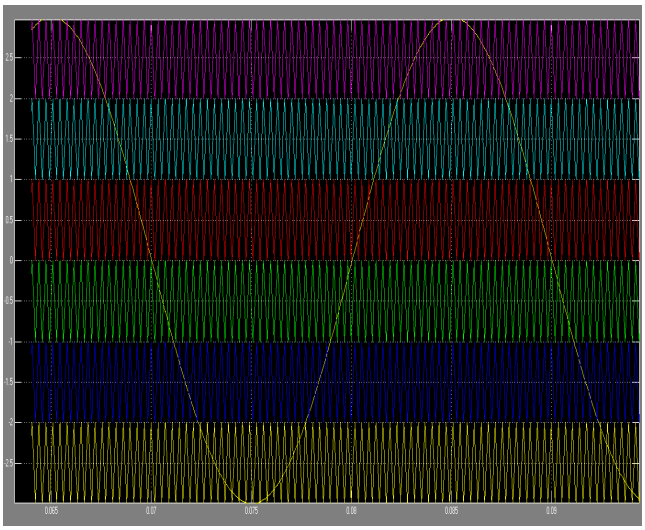

Fig.1.Reference and carrier waveform for PD CLSPWM

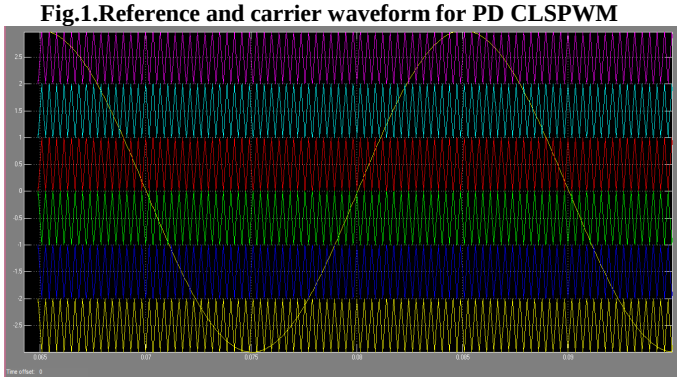

Fig.2.Reference and carrier waveform for POD CLSPWM

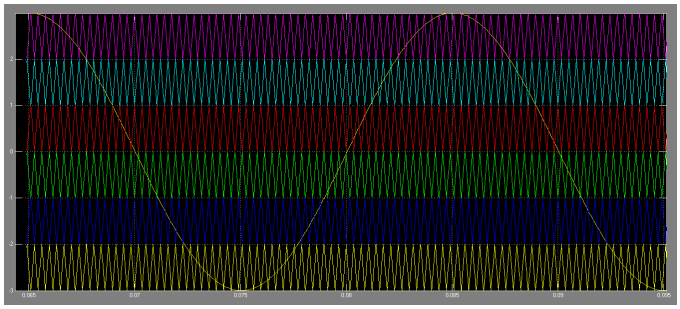

Fig. 3. Reference and carrier waveform for APOD CLSPWM

IV. STUDY CASE IMPLEMENTED IN MATLAB

The simulation of asymmetrical cascaded MLI is carried out using MATLAB/SIMULINK.it is shown in the fig.4.and fig-5

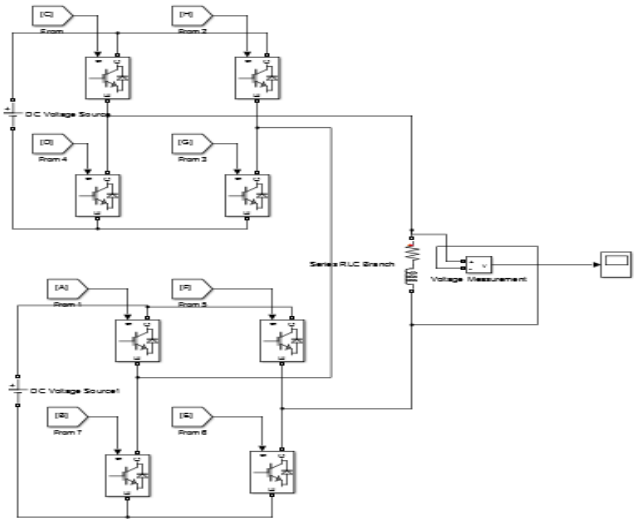

Fig.4. Simulation of single phase asymmetrical seven level inverter

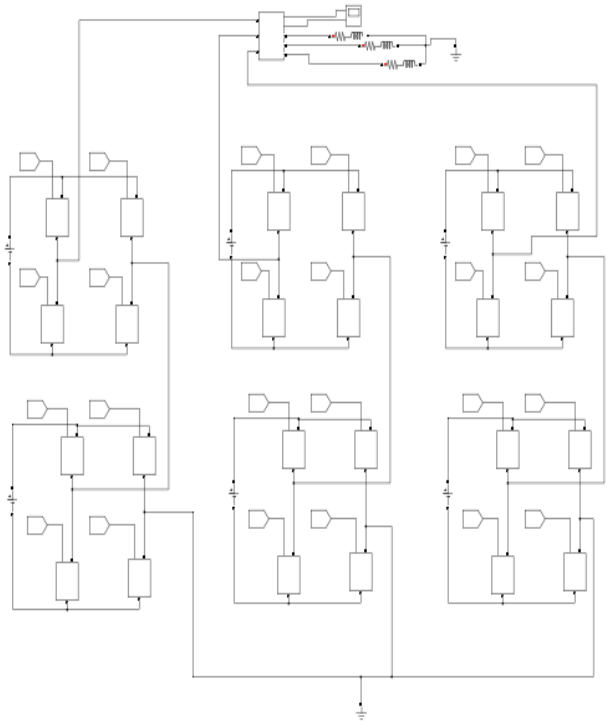

Fig.5. Simulation of three phase asymmetrical seven level inverter

The control circuit of asymmetrical cascaded MLI is same for both three phase multilevel inverter and single phase multiinverter .The dc source which we used is of different voltages because of asymmetrical cascaded h bridge multilevel inverterVdc1=105.3 volt,Vdc2=210.6 volt and voltage is shown in voltage measurement scope give the waveform in form of pulses it show 7 level inverter.

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Igbt are used in circuit for fast switching and at a time only one switch is on, means in one H-bridge two switch on and two switch off.

The switching pattern are same ,in these we are taken one sine wave and 6 carrier wave are used .for realizing SPWM a high frequency triangle carrier wave Vr is compare with a sinusoidal reference wave Vr of the desired frequency. The intersect of these two wave give the switching instant and commutation of modulated pulse the self commutation are done automatically it does not require manual operation .The high frequency carrier wave and the sinusoidal reference wave are mixed up in comparator. The comparator are used to compare the signal in the form of 0 or 1 .after these the signal goes to xor gate then in not gate and switch is on and the voltage flow in circuit and give 7 level multilevel inverter.

V. SIMULATIONS RESULTS

The output voltage waveform seven level asymmetric cascaded multilevel inverter with RL load for 5 cycles using CLSPWM is and its FFT analysis is shown in Fig.6 The same voltage waveform using POD-CLSPWM and its FFT analysis is shown in Fig.7. And using APODCLSPWM and its FFT analysis is shown in Fig.8.mainly we are reducing the THD less than 5% in both single phase multilevel inverter and three phase multilevel inverter.

THD analysis of single phase are given below

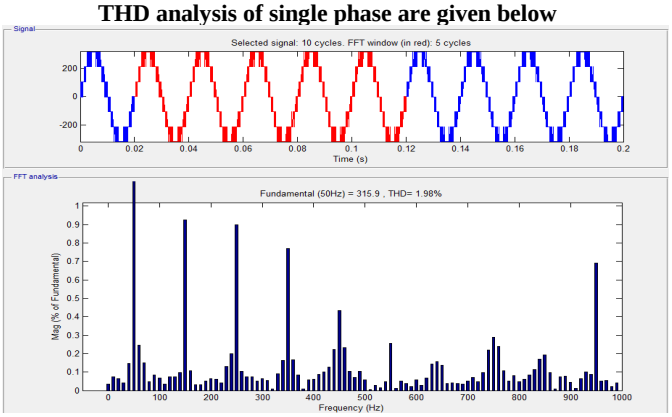

Fig-6 output phase voltage and FFT analysis of voltage waveform of cascaded multilevel inverter using PD CLSPWM

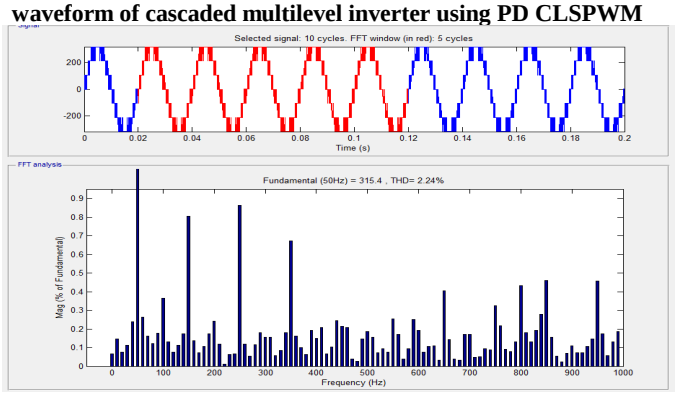

Fig-7- output phase voltage and FFT analysis of voltage waveform of cascaded multilevel inverter using POD CLSPWM

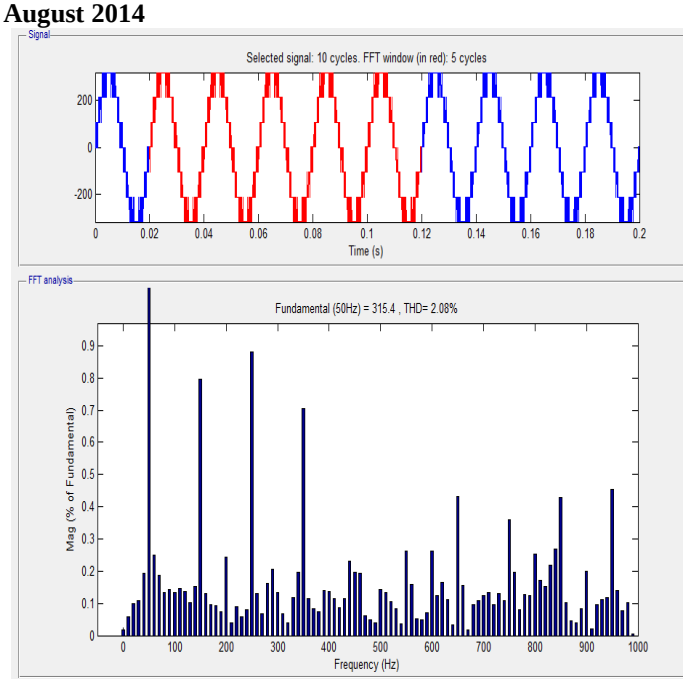

Fig 8- output phase voltage and FFT analysis of voltage waveform of cascaded multilevel inverter using APOD CLSPWM

Comparing THD of single phase PD,POD,APOD techniques

	PD	POD	APOD
THD	1.98	2.24	2.08

THD analysis of three phase multilevel inverter are given below-

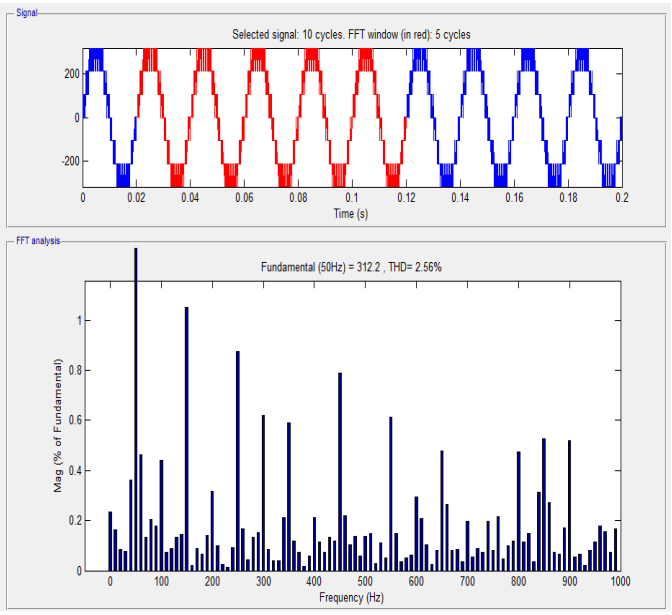

Fig-9 output phase voltage and FFT analysis of voltage waveform of cascaded multilevel inverter using PD CLSPWM

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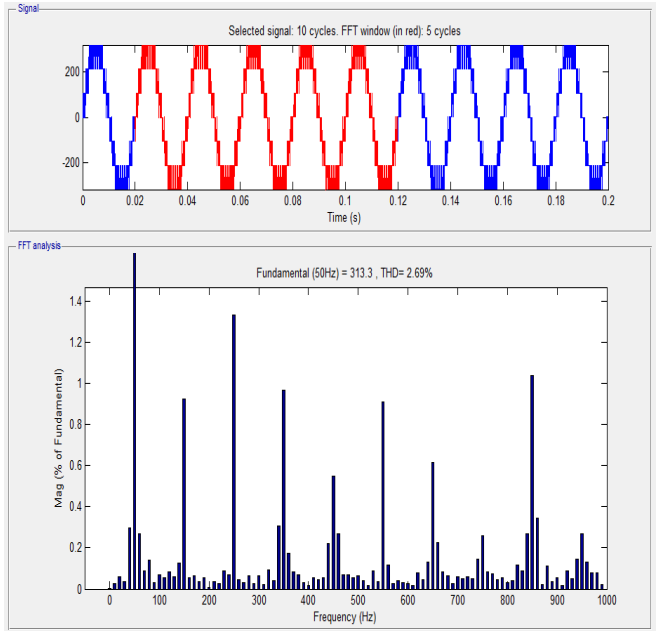

Fig-10 output phase voltage and FFT analysis of voltage waveform of cascaded multilevel inverter using POD CLSPWM

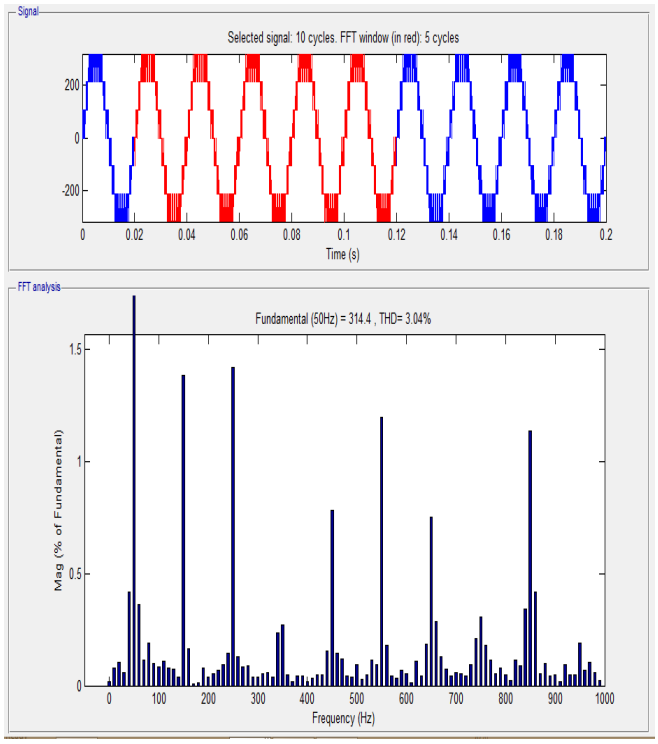

Fig-11 output phase voltage and FFT analysis of voltage waveform of cascaded multilevel inverter using APOD CLSPWM

Comparing THD of three phase PD, POD, APOD techniques

THD	PD	POD	APOD
1 PHASE	2.56	2.46	2.38
2 PHASE	2.69	2.20	2.27
3 PHASE	3.04	2.11	2.08

OUTPUT VOLTAGE OF SINGLE PHASE AND THREE PHASE MULTILEVEL INVERTER

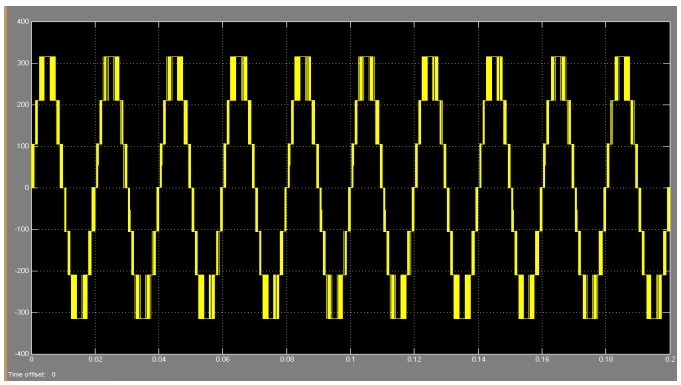

Fig 12-output voltage of single phase

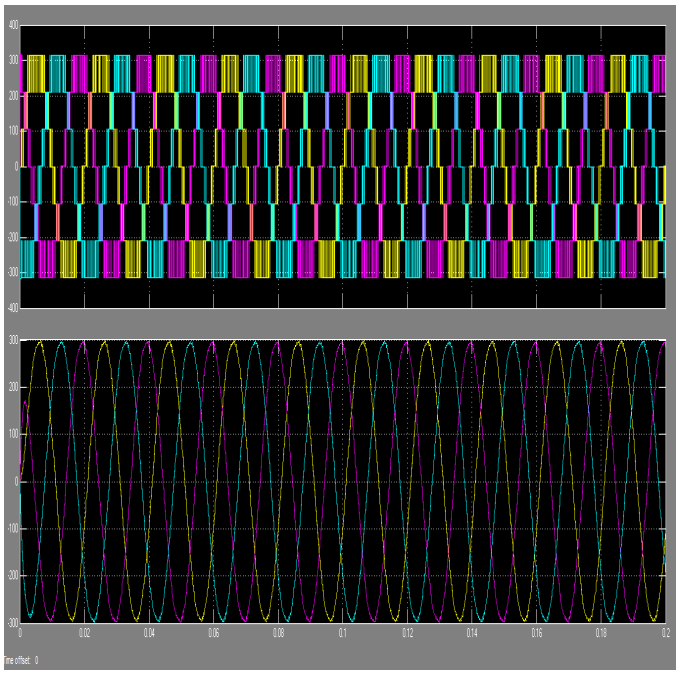

Fig 13-output voltage and current of three phase 7 level multilevel inverter.

VI. CONCLUSION

In asymmetrical topology the output voltage is seven level by using only 2 bridges (8 switches) where as symmetrical topology uses 3 bridges(12 switches).therefore the number of switches are reduced in asymmetrical topology compared to Symmetrical topology for the same no of levels. The THD of the voltage of asymmetrical CMLI is studied under different modulation techniques such as PD, APOD, POD and the less THD is observed for APOD technique.

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