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SiC Schottky barrier diodes studied by admittance spectroscopy

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Abstract:* The electrical properties of deep levels related to defects in real packaged SiC Schottky barrier rectifiers were studied by admittance spectroscopy (AS). The measurements were performed at temperatures ranging from 300 K down to 80 K and for frequencies between 2 kHz to 1 MHz. Rectifying properties of the diodes were studied by the measurement of the current-voltage (I-V) and capacitance-voltage (C-V) characteristics. Low temperature I-V characteristics exhibited large excess currents. AS spectra revealed three defect-related levels of activation energy equal to 0.17 eV, 0.23 eV and 0.36 eV. The results of present studies let us anticipate that the trap levels are responsible for the low-temperature excess current observed for the diodes.

Index Terms—**4H-SiC, Admittance Spectroscopy, deep-level defects, DLTS, I-V and C-V characteristics.**

I. INTRODUCTION

Silicon carbide (SiC) is a IV – IV semiconductor material with indirect bandgap. The most popular polytypes of SiC are 4H-SiC and 6H-SiC. Both have a wurtzite type crystal structure. The energy gap for SiC (at 300 K Eg = 3.0 ÷ 3.2 eV) is close to the energy gap of GaN (at 300 K Eg = 3.4 eV) and therefore it is widely used as an alternative to GaN. Silicon carbide has many applications in micro- and optoelectronics. The main driving force for increasing interest in SiC is hope that SiC-based power devices are promising candidates to high temperature, high frequency and high power applications. The factors favouring SiC for such applications have already been widely argued: high breakdown field, low leakage current, high Schottky barrier height, high thermal conductivity, etc. Recently, SiC has been seriously considered as a valid alternative to silicon for the production of radiation hard ionizing particle detectors. With respect to all these applications the study of defects present in the devices based on SiC has crucial importance for their operation. In spite of the fact that the market for SiC-based devices is developing rapidly there are still unsolved problems with defects deteriorating their performance. The most exploited technique used to investigate and characterize deep level traps in semiconductors is the deep level transient spectroscopy (DLTS) method. However if a deep level cannot follow the high frequency voltage modulation (DLTS is usually based on a 1 MHz capacitance bridge) this technique fails. Admittance spectroscopy (AS) is an alternative technique enabling studies of electrical properties of defect - related levels even in the case of slow traps. The motivation of this work were the results reported at [1]. It was found that some of the commercially available SiC diodes exhibited large excess currents in specific ranges of forward and reverse current–voltage characteristics. It was proposed that such behavior may be due to the presence of defects. In our recent paper [2] we have analyzed the Schottky barrier inhomogeneity in these diodes. DLTS measurements revealed the presence of a trap located close to the interface SiC-metal presumably responsible for the observed inhomogeneity and undesired excess current. In this paper the I-V characteristics were analyzed again but by using the approach proposed by Horvath [3]. This method is particularly useful for the diodes exhibiting large excess current. Moreover, our studies on defects in these diodes were extended by using another experimental method, the admittance spectroscopy, as an alternate to the DLTS technique. As a result, beside the trap observed in DLTS, two new traps were detected. Additionally, Raman measurements confirmed that the studied diodes are 4H-SiC based.

II. EXPERIMENT

Four commercial SiC Schottky barrier rectifiers produced by Cree Inc. were studied in this work. The rectifiers CSD01060 (1 A, 600 V) have typical packages TO-220-2 and are applied in switch mode power supplies, power factor correction and motor control [4]. In order to identify the polytype of the SiC (4H or 6H) room temperature Raman spectroscopy measurements were performed for one of the diodes by using a T64000 Jobin Yvon spectrometer operating in a single mode with a liquid nitrogen-cooled charge-coupled device detector. The spectrum was obtained in the backscattering geometry, with an excitation of the 514 nm Ar+ laser line. Current-voltage characteristics were measured within the 77 K – 380 K range of temperature with the use of Keithley 2601 I-V source–meter. The capacitance-voltage C-V and admittance spectroscopy measurements were performed with the use of Novo control Impedance Analyzer within temperature ranging from 80 K up to 300 K and frequency range from several kHz up to 3MHz. The most important problem of this research is the fact that we have studied real-packaged SiC Schottky diodes with almost no information about the area and kind of metallization used for

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preparation of the Schottky contact, as well as the type and doping level, and also the kind of polytype of the used SiC material. This is essential for proper analysis of electrical characteristics and calculation of diode parameters. Therefore, in this research we assumed the junction area equal to 0.5 mm^2, which in our opinion is close to the typical values used for SiC Schottky diodes. Indeed, we obtained electrical parameters (especially SBHs) close to the typically observed for 4H-SiC Schottky barrier rectifiers with different metallization's [2].

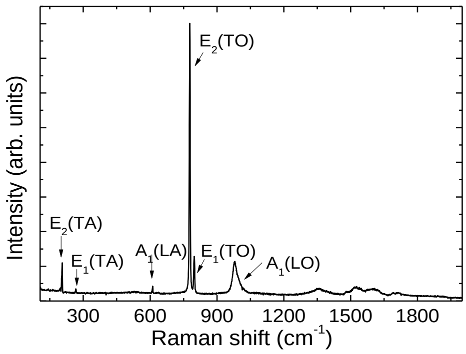

Fig.1. Room temperature Raman spectra excited with the Ar2+ laser line of 514 nm. The labels correspond to the related phonon modes [4,5].

III. RESULTS

Firstly, we had to resolve the problem of the SiC polytype used to produce the studied Schottky diodes. For this purpose the Raman spectroscopy measurements for one of the diodes (after destruction of its housing) were performed. Resulting Raman spectra are shown in Fig. 1. The Raman peaks observed in the figure have been compared with the phonon modes for 4H-SiC and 6H-SiC [5,6]. Their positions agree very well with the Raman spectra of 4H-SiC. In particular the peak at 100 cm^{-1} corresponds to the E2(TA) mode in 4H-SiC [5,6]. This mode in 6H-SiC should appear at 150 cm^{-1} (not observed in Fig. 8). Similarly, the A1(LA) mode for 4H-SiC corresponds to 609 cm^{-1} (as in Fig. 8) whereas the same mode for 6H-SiC should be observed at 505 cm^{-1} (missing in Fig. 8). Thus we may conclude that the studied samples are Schottky diodes based on 4H-SiC (what was also confirmed

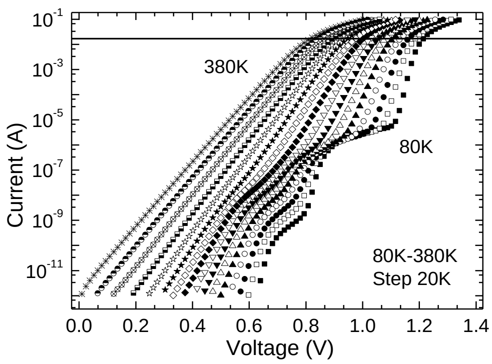

Fig. 2 Current–voltage characteristics of a SiC Schottky barrier diodes as a function of temperature, exhibiting excess

currents at low temperatures and biases, and saturation at high current levels due to series resistance. The horizontal line indicates a current level of 17 mA attributed to thermionic emission at each temperature. in personal communication with Cree Inc. representatives). Rectifying properties of the diodes were studied by standard I-V method. Fig. 2 shows representative I-V characteristics in a semi-logarithmic plot for one of the studied diodes at several temperatures within the range of 80 K – 380 K. At 380 K at a voltage bias up to 0.8 V the ideality factor is close to 1, yielding thermionic emission (TE) mechanism of current transport through the Schottky junction. At lower temperatures however the TE mechanism is hardly to be distinguished for increasing contribution of excess current (i.e. an additional current over the current attributed to the Schottky junction yielding linear lnI - V relation at low current density). The analysis of the characteristics performed in our recent paper lead us to the conclusion that in these diodes there are two, low and high Schottky barriers (SB), equal to about 1.17 eV and 1.3 eV, respectively [2]. The low SB is due to the existence of local defective patches surrounded by large area contact regions with high SB. In the present paper, in order to extract the junction parameters based on the characteristics disturbed by the excess current (and series resistance), a method proposed in [3] was applied. Through an ideal Schottky junction the TE current is given by equation [7]:

$$I = AA^{*}T^{2}\exp\left(\frac{-q\Phi_b}{kT}\right)\exp\left(\frac{qV}{kT}\right) \qquad (1)$$

where A is the junction area, A^* – effective Richardson constant, q – the elementary charge, Φ_b – barrier height. The ideality factor a is assumed to be equal to 1. For an actual value of current I_1 and taking the logarithm of both sides, after rearranging Eq. (1) one obtains [3]:

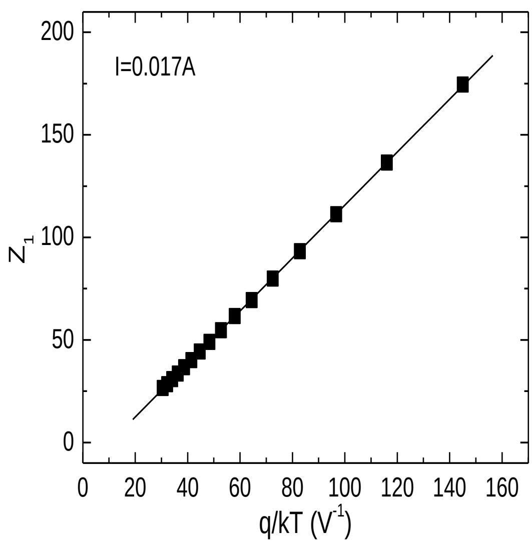

Fig. 3. Z_1 plots obtained from the I–V characteristics of SiC Schottky barrier diodes presented in Fig. 2, respectively, by using Eq. (2) for the actual current level I_1 of 17 mA. Line is linear fit to the experimental points.

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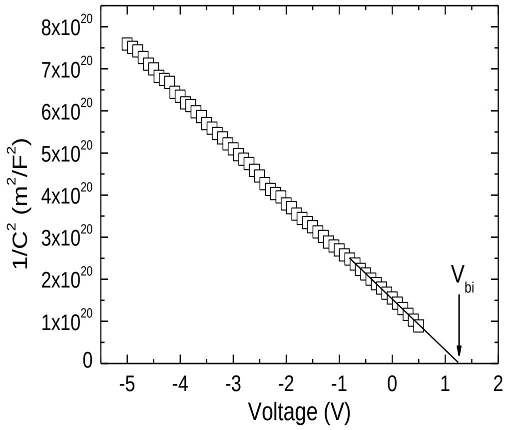

Fig. 4. The capacitance–voltage characteristics of SiC Schottky barrier diodes measured at 360K (at 1 MHz).

$$Z_1 \equiv \frac{qV}{kT} + \ln AT^2 - \ln I_1 = -\ln A^* + \frac{q}{kT}\Phi_b \qquad (2)$$

with voltage V corresponding to the value of I_1. A plot of Z_1 versus q/kT is a straight line. Its slope yields barrier height whereas its Z_1 intercept – the effective Richardson constant. Z_1 plots obtained from the I-V characteristics of the studied SiC diodes shown in Fig. 2 by using Eq. (2) for the actual current I_1 of 17 mA (with the assumption that junction area equals 0.5 mm^2) are presented in Fig. 3. Barrier height Φ_b, determined from the slope, equals to 1.29 eV. This value is close to the high SB obtained by us earlier [2]. Effective Richardson constant extracted from the Z_1 versus q/kT plot equals to 67 A/cm^{2}K^2. This value is twice less than 146 A/cm^{2}K^2 , the value expected for 4H-SiC [8], but this discrepancy is due to the fact that the exact value of a Schottky junction area is missing. On the other hand, it should be noted that the value of area does not affect the value of barrier height determined by this method.

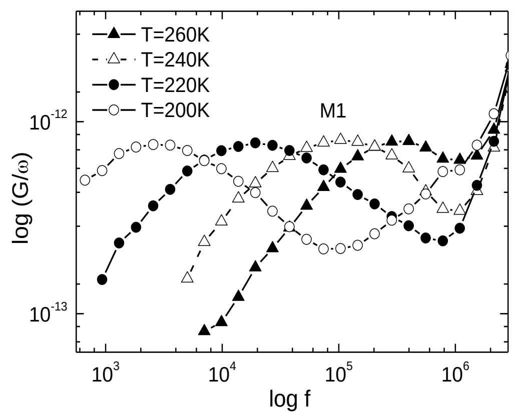

Fig. 5. Conductance divided by frequency vs frequency (FAS mode of AS operation) measured at different temperatures. Steady-state applied voltage is V=0V.

Fig. 4 shows $1/C^2$ versus bias V curve measured at 360 K (at 1 MHz). From the linear fit of the plot the built-in voltage V_{bi} of 1.21 eV is obtained. This value is less than barrier height in accordance with expected relationship between both [7]:

$$q\Phi_b = qV_{bi} + qV_n + kT \qquad (3)$$

Exact value of qV_n, i.e. the distance of Fermi level from the conduction band edge, cannot be determined from the $1/C^2$ versus bias V plot for the lack of information on the exact value of the area A of the junction. However assuming values of donor doping carrier concentration N_D between 10^{15} cm^{-3} and 10^{16} cm^{-3}, typical for commercially available SBD [9], the value of qVn can be estimated using the well-known formula:

$$qV_n = kT \ln \frac{N_c}{N_D} \qquad (4)$$

with $N_c = 3.25 \times 10^{15} \times T^{3/2}$ cm^{-3} for 4H-SiC [8]. For the lower doping level it equals 0.29 eV and for higher – 0.2 eV for 4H-SiC. Eventually the barrier height determined from Eqs. (3) and (4) is higher (~1.3 eV – 1.5 eV) than that obtained based on I-V characteristics. It is worth noting however, that barrier heights calculated from CV data are often somewhat higher than barrier heights extracted from IV data taken from the same diode. Bhatnagar et al. [10] proposed a model to explain these behaviors in which localized surface defects, perhaps elementary screw dislocations where they intersect the SiC-metal interface, cause locally reduced junction barriers in the immediate vicinity of the defects. Because current is exponentially dependent on the Schottky barrier height, this results in the majority of measured current flowing at local defect sites instead of evenly distributed over the entire Schottky diode area.

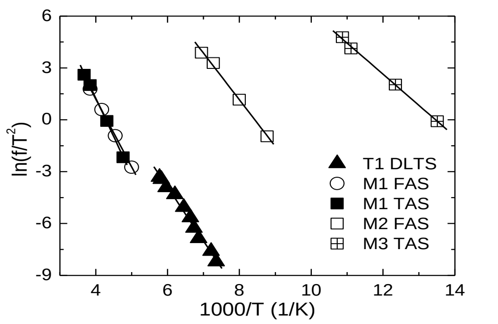

Fig. 6. Arrhenius plot obtained from the evolution of the peaks with temperature. The Arrhenius plot obtained from DLTS studies [2] was also shown for comparison.

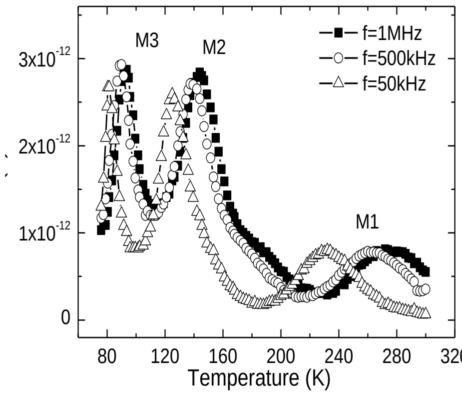

Fig. 7. Conductance divided by frequency vs temperature (TAS mode of AS operation) measured at different frequency. Steady-state applied voltage is V=0V.

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Admittance spectroscopy (AS) indeed gives direct access to the emission – capture processes occurring between an impurity level and the conduction or the valence band [11]. A defect state in the band gap leads to a decrease of capacitance and an appearance of the peak in the curves of conductance/frequency versus frequency at different temperatures (FAS – frequency admittance spectroscopy) or conductance/frequency versus temperature at different frequencies (TAS – thermal admittance spectroscopy). Through the temperature dependence of the position of this peak, the energy activation level can in principle be deduced from corresponding Arrhenius plot like in the ordinary DLTS analysis. In present study in the FAS mode, the conductance (G) was monitored within the frequency range of 500Hz to 3MHz and for temperature between 100K – 300 K. The conductance G divided by $\omega=2\pi f$, where f is the ac-signal probe frequency, was measured at different voltage bias. The results of FAS measurements at zero dc voltage bias are shown in Fig. 5. For the temperature in the range from 200 K to 260 K the G/ω curves show a single relaxation maximum labeled by us as M1.

Table I. Activation energies (E_a) and apparent capture cross sections (σ_a) of the traps revealed in 4H-SiC diodes by means of DLTS [2], FAS and TAS methods.

Trap	T1 DLTS	M1 FAS	M1 TAS	M2 TAS	M3 TAS
E_a (eV)	0.3	0.34	0.36	0.23	0.17
σ_a (cm^2) 4H SiC m*=0.37m$_0$ [5]	7.4 ×10^{-15}	6.2 ×10^{-15}	2.0 ×10^{-14}	1.2 ×10^{-12}	6.7 ×10^{-11}

The maximum is not sensitive to the reverse bias. From the evolution of the peak with temperature Arrhenius plot (Fig. 6) was constructed, i.e. the relation of $\ln f/T^2$ vs $1000/T$, where f stands for the frequency at a temperature T_{max} corresponding to the peak position in the FAS spectrum. Apparent activation energy, i.e. energy level distance from the conduction band edge and apparent capture cross section of the trap determined with the help of related Arrhenius plot are equal to 0.34 eV and 6.2 × 10^{-15} cm^2, respectively. In the TAS mode of AS operation, the position of the dispersive peak as a function of temperature was measured at different frequencies. The conductance was monitored as a function of temperature from 20 K to 300 K. These measurements were made at three different frequencies: 50 kHz, 500 kHz and 1 MHz and for different reverse bias. Fig. 7. Shows results of TAS measurements at zero dc bias voltage. The conductance divided by ω versus temperature plot exhibits three peaks. These peaks are labeled as M1, M2 and M3. The activation energies of related deep levels calculated from Arrhenius plots shown in Fig. 5 are equal to 0.36 eV for M1, 0.23 eV for M2 and 0.17 eV for M3. The apparent capture cross sections of the traps M1, M2 and M3 are collected in Table I. As it was mentioned in the introduction, DLTS studies performed for the studied diodes yield a single maximum (labeled by us T1 [2]). Arrhenius plot of a deep level associated with this peak, also included in Fig. 6, yields apparent activation energy and capture cross section equal to 0.3 eV and 7.4 × 10^{-15} cm^2 [2]. Comparison of the Arrhenius plots collected in Fig. 6 let us conclude that the trap T1 determined from DLTS studies is the very trap M1 observed in FAS and TAS spectra. Both, signatures and locations on the Arrhenius plot are close, implying the same trap. Additionally, two traps are found with TAS measurement. It has to be underlined that so far there were no reports on a deep level of activation energy equal to 0.3 eV in 4H-SiC, whereas defect level of close signature was detected for 6H-SiC [12]. We have not observed also the so-called defect Z1, commonly observed for 4H-SiC [13] In our paper on DLTS studies performed for the diodes we have assumed that the trap of energy 0.3 eV was responsible for the observed low-temperature excess current [2]. However from the present AS studies it is clear that the highest TAS and FAS signals exhibit the traps of the lower energy (cf. Fig. 7). Thus the concentration of the defects related to these traps is higher than the concentration of the defects linked with the 0.3 eV trap. The results of present studies let us anticipate that these levels also participate in the mechanism of the low-temperature current transport in the studied diodes. It is possible that these defects are too slow to be observed by means of DLTS measurements. As it is clearly seen, in spite of the fact that the technology of the 4H-SiC Schottky diodes is matured there are still some unsolved problems linked with the presence of defects. The authors hope that obtained results would shed light on the problem of defects in the diodes. In the near future, we plan to expand our electrical measurements (DLTS, AS) into a higher temperature range, where much more electrically active defects are usually observed in the wide bandgap 4H-SiC.

IV. CONCLUSION

In the paper, rectifying properties of SiC Schottky diodes were analyzed by I-V and C-V measurements, within a wide range of temperature. Raman measurements revealed that the studied diodes were 4H-SiC based. Low temperature I-V characteristics exhibited large excess currents and therefore they were analyzed by using a method invented by Horvath [3], especially designed for such diodes. Based on the I-V characteristics, the value of Schottky barrier height was found (1.3 eV) to be somewhat less than the barrier determined from the C-V measurements (1.5 eV). Thermal admittance spectroscopy and frequency admittance spectroscopy were used to characterize the trap levels related to defects in these diodes. Three traps of apparent activation energy equal to 0.17 eV, 0.23 eV and 0.36 eV were detected by using the TAS method and a single trap of signature close to the 0.34 eV trap by using FAS technique. It was also found that the concentration of the defects related to these traps is higher than the concentration of the defects linked with the highest energy trap. The results of present studies let us anticipate that the energy levels are responsible for the low-temperature excess current observed for the diodes.

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REFERENCES

[1] Z. Synowiec, “SiC Schottky barrier rectifiers – theory and practice”, Mater. Electron. vol. 32, pp. 5-22, 2004.

[2] Ł. Gelczuk, P. Kamyczek, E. Płaczek-Popko, and M. Dabrowska-Szata, “Correlation between barrier inhomogeneities of 4H-SiC 1A/600V Schottky rectifiers and deep-level defects revealed by DLTS and Laplace DLTS”, Solid State Electronics, vol. 99, pp. 1-6, April 2014.

[3] Zs. J. Horvath, “Evaluation of Schottky junction parameters from current-voltage characteristics exhibiting large excess currents”, Appl. Surf. Sci., vol. 255, pp. 743-745, July 2008.

[4] www.cree.com/~/media/Files/Cree/.../CSD01060.pdf.

[5] J. C. Burton, L. Sun, M. Pophristic, S. J. Lukacs, F. H. Long, Z. C. Feng, and I. T. Ferguson, “Spatial characterization of doped SiC wafers by Raman spectroscopy”, J. Appl. Phys., vol. 84, pp. 6268–6273, December 1998.

[6] J. C. Burton, L. Sun, F. H. Long, Z. C. Feng and I. T. Ferguson, “First- and second-order Raman scattering from semi-insulating 4H−SiC”, Phys. Rev. B, vol. 59, pp. 7282–7284, March 1999.

[7] S. M. Sze, and K. Ng. Kwok, “Physics of Semiconductor Devices”, Wiley-Interscience, 2006.

[8] http://www.ioffe.ru/SVA/NSM/Semicond/SiC/index.html.

[9] http://www.iue.tuwien.ac.at/phd/ayalew/mythesis.html.

[10] M. Bhatnagar, B. J. Baliga, H. R. Kirk, and G. A. Rozgonyi, "Effect of Surface Inhomogeneities on the Electrical Characteristics of SiC Schottky Contacts," IEEE Trans. Electron Devices, vol. 43, pp. 150-156, January 1996.

[11] P. Blood, and J. W. Orton, “The electrical characterization of semiconductors: majority carries and electron states”, Academic Press, London, 1990.

[12] N. I. Kuznetsov, and J. A. Edmond, “Effect of deep levels on current excitation in 6H-SiC diodes”, Semiconductors, vol. 3, pp. 1049-1052, October 1997.

[13] T. Dalibor, G. Pensl, H. Matsunami, T. Kimoto, W. J. Choyke, A. Schöner, and N. Nordell, “Deep Defect Centers in Silicon Carbide Monitored with Deep Level Transient Spectroscopy”, Phys. Stat. Sol. (a), vol. 162, pp. 199-225, January 1997.

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