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Field Programmable Gate Array Based Intelligent Traffic Light System

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Abstract*— The use of FPGAs (Field Programmable Gate Arrays) and configurable processors is an interesting new phenomenon in embedded systems development. FPGAs offer all of the features needed to implement most complex designs. In this paper, a real time traffic light controller, based on the FPGA was designed, with the Finite State Machine and clock timer at its heart. The design has several benefits over ordinary traffic light systems built with microcontrollers or Programmable logic controllers, such as simple structure, high reliability, and re-configurability for upgrades. The FPGA based intelligent traffic light system is capable of achieving optimal traffic signal settings at signalized intersections such that vehicle delay times, stops, and queue lengths are minimised. A four way junction with intersecting roads named; North, East, South and West, was considered. With the aid of sensors, the FPGA responds appropriately by cutting off roads with no vehicles and allowing traffic to flow along others in order of priority. The coding of the design was done using VHDL, and the design was tested and simulated on the Xilinx Spartan-6 LX16 FPGA, after which a model of the system was constructed.

***Index Terms*—FPGA, Intelligent Traffic Light System, State Machine, VHDL, Xilinx ISE.**

I. INTRODUCTION

The traffic on our roads, especially intra-city traffic, due to increasing number of cars grows by the day and unless adequate steps are taken to control the situation, we shall soon have some serious problems that may affect economic growth. The existing methods for traffic management, surveillance and control are not adequately efficient in terms of the performance, cost, and the effort needed for maintenance and support. The use of FPGAs (Field Programmable Gate Arrays) and configurable processors is an interesting new phenomenon in embedded development. FPGAs offer all of the features needed to implement most complex designs. Clock management is facilitated by on-chip PLL (phase-locked loop) or DLL (delay-locked loop) circuitry. Dedicated memory blocks can be configured as basic single-port RAMs, ROMs, FIFOs, or CAMs. Data processing, as embedded in the devices' logic fabric, varies widely. The ability to link the FPGA with backplanes, high-speed buses, and memories is afforded by support for various single ended and differential I/O standards. Also found on today's FPGAs are system-building resources such as high speed serial I/Os, arithmetic modules, embedded processors, and large amounts of memory [1]. FPGAs are preferable to conventional microcontroller devices for many reasons. First, programming data is not lost when they are exposed to light. This ensures a longer lifespan of whatever system they control especially if they are placed in an external environment. A single FPGA can control multiple processes concurrently as well as sequentially. This leads to better efficiency, lower cost and reliability of the system. Real time control of Traffic signals can be achieved easily without including external components as in the case of microcontrollers, which leads to higher costs. According to [2]; "The system has several benefits over ordinary traffic light controllers such as simple structure, high reliability, low costs, easy installation and maintenance". This statement was made because he was able to implement an FPGA based traffic controller for five intersecting main roads with minimum resource usage. It is interesting to note that the FPGA can have up to 64 logic states (i.e. 64 individual output ports), and his design requires only 25 logic states leaving enough room for other operations. Comparing this with that of the traffic light controller designed by [3], for a T-junction, we can see that the microcontroller resources were stretched thin and in order to control a larger traffic light system, more controllers may be required which will increase system cost and complexity. This paper was aimed at designing and implementing a FPGA based traffic light system, capable of detecting the presence of vehicles at each oncoming lane and then reacting appropriately to improve traffic flow by reducing wait time.

A 4-way road junction was considered with infrared sensors placed at each oncoming lane, as shown in Fig 1. If a vehicle is detected on one lane, the traffic signal for that lane turns green, while the others turn red; hence only one lane's traffic is allowed to flow during each traffic phase. When no vehicles are detected, only the red traffic lights come on. Otherwise, the North traffic will be allowed to move, followed by the traffic in the East, South and then the West direction. If some roads do not have vehicles present at the intersection then their corresponding traffic lights will be cut off from the traffic cycle. Fig 2 shows a flow chart describing the Traffic algorithm to aid in better understanding the system. When all 4 roads at the intersection are empty, the red traffic signal is turned on for all lanes.

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I. DESIGN

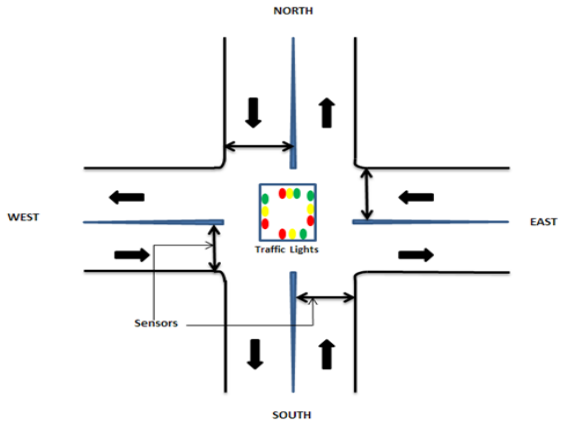

Fig 1: Model of a 4 Way Junction

Whenever a vehicle is detected on a road, the green traffic signal for that road comes on. In this design, the North has the highest priority followed by the East, South then West. The timing for each traffic phase can easily be adjusted when necessary, to suit traffic needs on each lane. The traffic light controller for the specifications given will require two major components: a state machine to keep track of the current state of the traffic and the next state that the traffic should enter into; and a counter which will control when the transitions from one traffic state to another occurs. These will be designed as two separate entities and then combined into one entity after tested. The final design is shown in fig 3. The sensors provide digital inputs to the Finite State Machine (FSM) of the FPGA. The FSM then responds appropriately with a delay time given by a specific count period which is derived with the aid of a clock divider that simply reduces the overall frequency of the system. The buffer stores the FSM outputs until the required delay time passes.

A. State Machine Design

From the specifications above, a state machine consisting of 9 states was designed. Details of each state are shown in Table I.

Table I: States of Intelligent Traffic Light System

State	State Description	NORTH	EAST	SOUTH	WEST
S_0	All red signals on	Red	Red	Red	Red
S_1	NORTH green	Green	Red	Red	Red
S_2	EAST green	Red	Green	Red	Red
S_3	SOUTH green	Red	Red	Green	Red
S_4	WEST green	Red	Red	Red	Green
S_5	NORTH yellow	Yellow	Red	Red	Red
S_6	EAST yellow	Red	Yellow	Red	Red
S_7	SOUTH yellow	Red	Red	Yellow	Red
S_8	WEST yellow	Red	Red	Red	Yellow

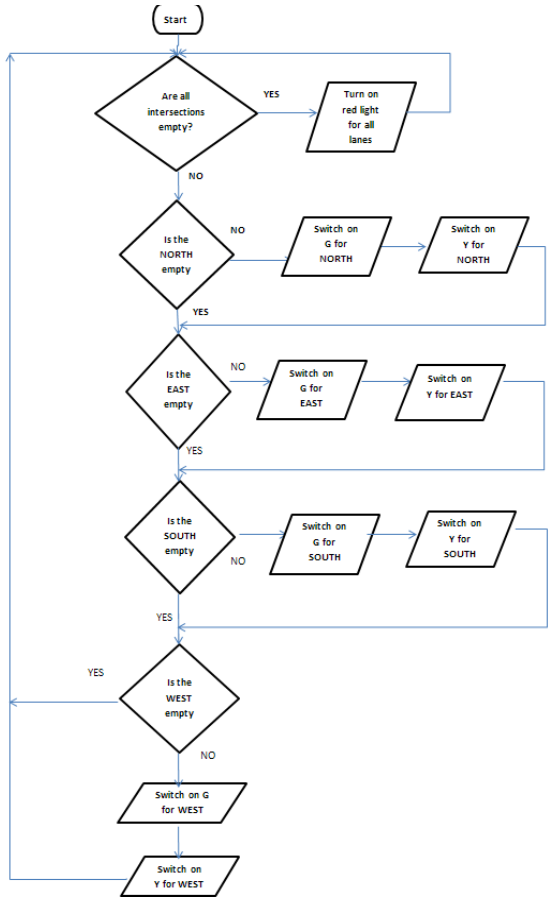

Fig 2: Intelligent Traffic Light Controller Flow Chart

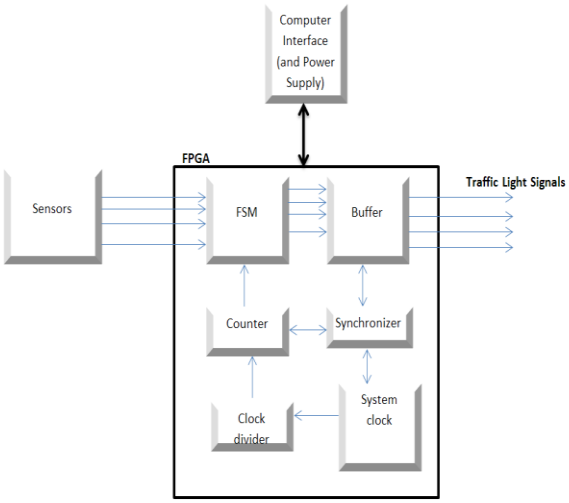

Fig 3: System Block Diagram

Two timing parameters were considered;

- timeG: refers to length of time green traffic signal will stay on.
- timeY: refers to length of time yellow traffic signal

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stays on.

These two parameters can easily be varied in order to suit traffic needs. In fact, more timing parameters can be included easily, but for demonstrative purposes only these two were used, with timeG set at 20 seconds and timeY set at 2 seconds.

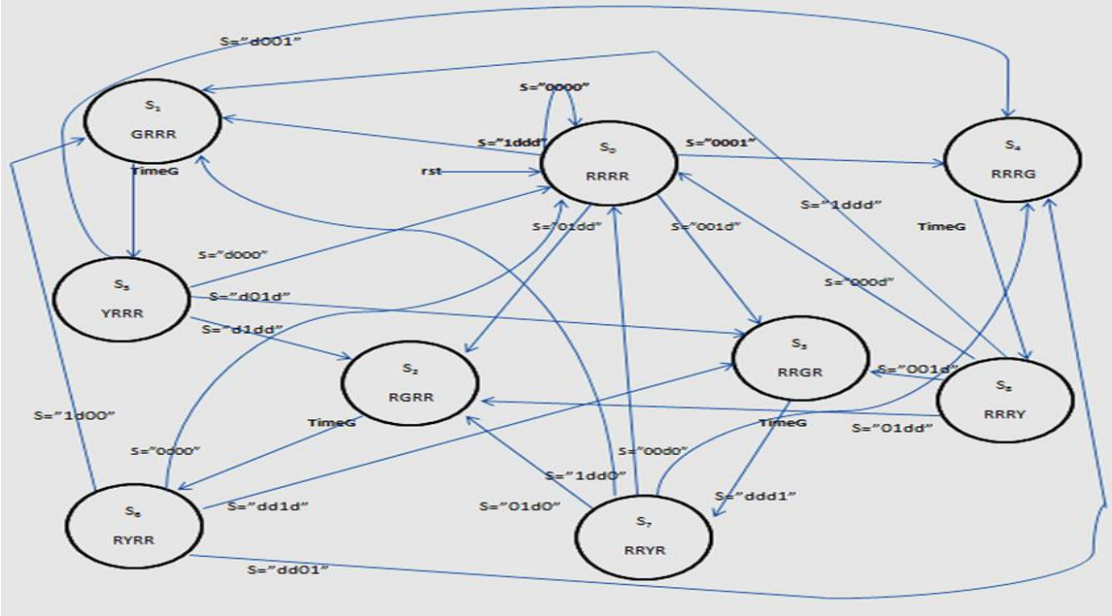

Fig 4: System State Machine

The sensor inputs to the FPGA from each road were represented as 4 bit binary vectors S="dddd", where'd' refers to 'don't care'. The MSB represents the sensor output from the North road (N_S); the next bit represents the sensor at the East (E_S), then the sensor at the South (S_S), with the LSB representing the sensor at the West (W_S). From fig 4, it can be observed that whenever all roads are empty, the system signals red lights in all 4 directions given by state S_0. Whenever cars arrive at the intersection, the system begins the traffic cycle starting with roads at higher priorities. The North road was designed to have the highest priority, followed by the East, South, and then West. Assuming 3 cars, from North, East and West arrive simultaneously at the junction. N_S, E_S and W_S will send signals to the FPGA. Since N_S has the highest priority, the system will change from S_0 to S_1, where the traffic light is green for the North road. It will stay in this state for a given timeG after which it would change to S_5, with the yellow signal displayed. It remains in S_5 for timeY before changing to state S_2, to begin the traffic phase of the East road, passing through states S_2 and S_6 before changing to state S_4 for the West road.

A simple infrared sensor was used to give logic 1 when a vehicle is present and logic 0 when the road is empty. If the IR LED emissions become incident on the phototransistor, the phototransistor's resistance comes down to a finite value. This reduces the voltage drop across the phototransistor, taken as input into the comparator, which is compared with the threshold given by the voltage drop across the variable resistor 'R_{V1}'.

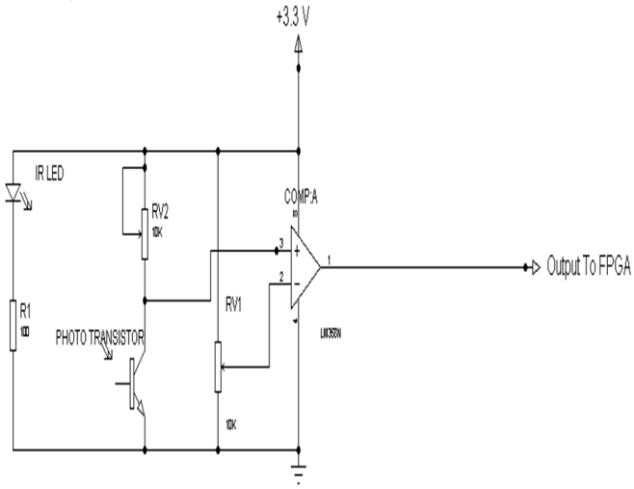

Fig 5: Sensor Circuit

The point to be noted here is that the more the incident radiation on the phototransistor, the lower the voltage drop across it, and hence more voltage will be dropped across R_{V2}. If the voltage developed across the phototransistor is greater than the set threshold voltage, the output of the comparator

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will be high, else it will be low. The 3.3 V DC is supplied by the FPGA. LM 358N DIP Op- amp was used as a comparator in order to give a logic output that can be interpreted by the FPGA. The Op-amp IC was selected because of its low power requirements. The Variable resistors R_{V1} and R_{V2} serve to vary the sensitivity of the sensor, in order to reduce the effects of ambient light. Reducing R_{V2} will lead to an increase in the voltage drop across the phototransistor, i.e. it makes the sensor less sensitive. Reducing the value of R_{V1} will reduce the threshold voltage, which will also reduce sensitivity to ambient light. R_1 is a limiting resistor for the IR LED. Its value was derived from the expression;

$$R_1 = \frac{V_+ - V_f}{I_f}$$

Where IR LEDs have a typical forward voltage drop of about 1.28 V and the forward current flow from the FPGA was 20 mA.

II. RESULTS

The Traffic light system was built using VHDL (Very High Speed Integrated Circuit Hardware Description Language) on the Xilinx ISE 14.1 CAD environment and the Quartus II software. After compiling the code, The Register Transfer Language (RTL) schematics as well as a state diagram were automatically generated.

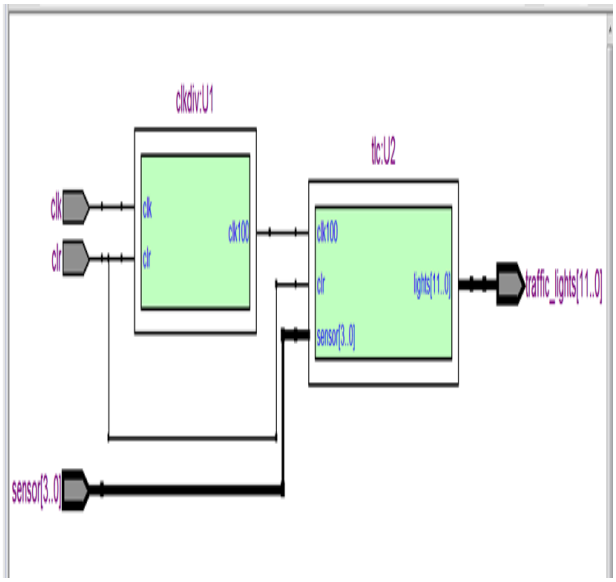

Fig 6: RTL view of intelligent traffic light system

The RTL schematic in figure 6 matches the overall system design shown. The clock divider (clkdiv) divides the main system clock to generate a 100 Hz clock which is fed into the state machine (tlc) for use as a counter. Also, the generated state diagram also matches the initial design state diagram shown in fig 4.

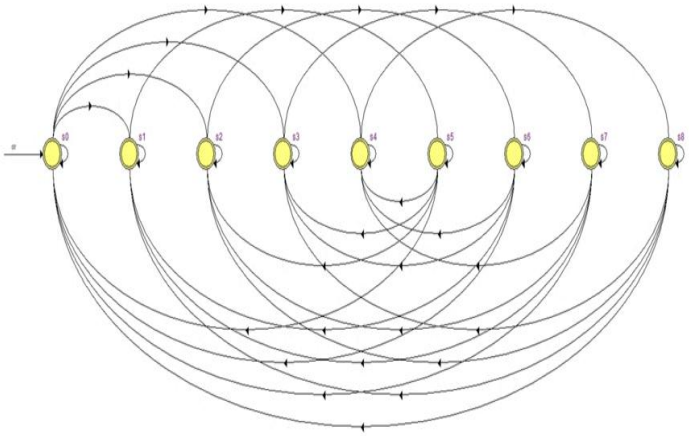

Fig 7: Simulated State Diagram

A) Functional Simulations

The following are functional simulations of the intelligent traffic light system taken after synthesis with the aid of a vector waveform file (VWF) that was generated using quartus, in order to observe the transitions of the system with varying inputs. To prevent the simulation from taking an unreasonable time to finish, timeG was reduced to 0.2 µS and timeY to 0.03 µS.

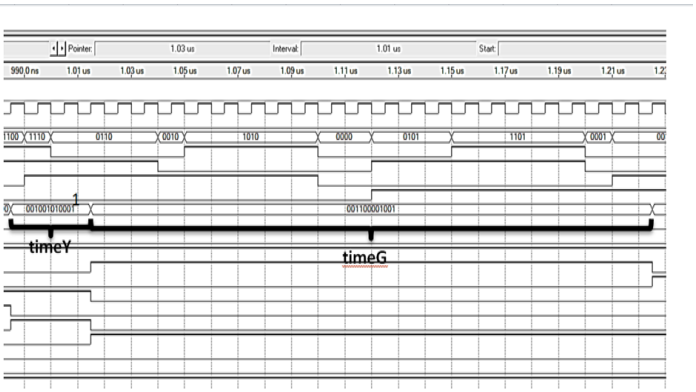

Fig 8: Time Periods of timeG and timeY

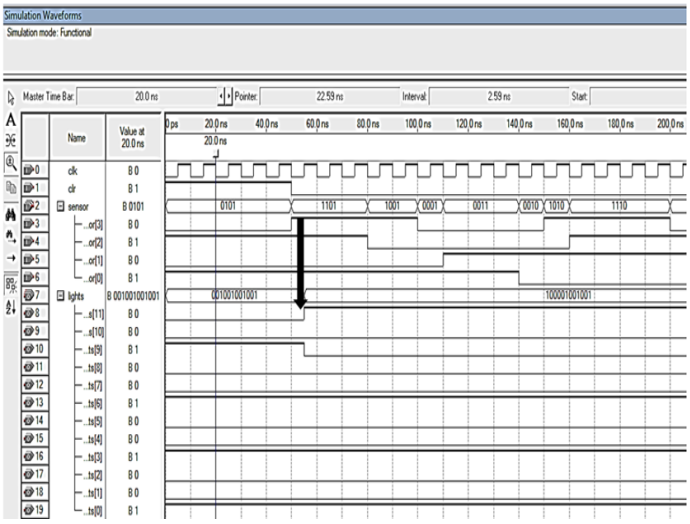

Fig 9: Simulation Behavioral Model When N_S is high

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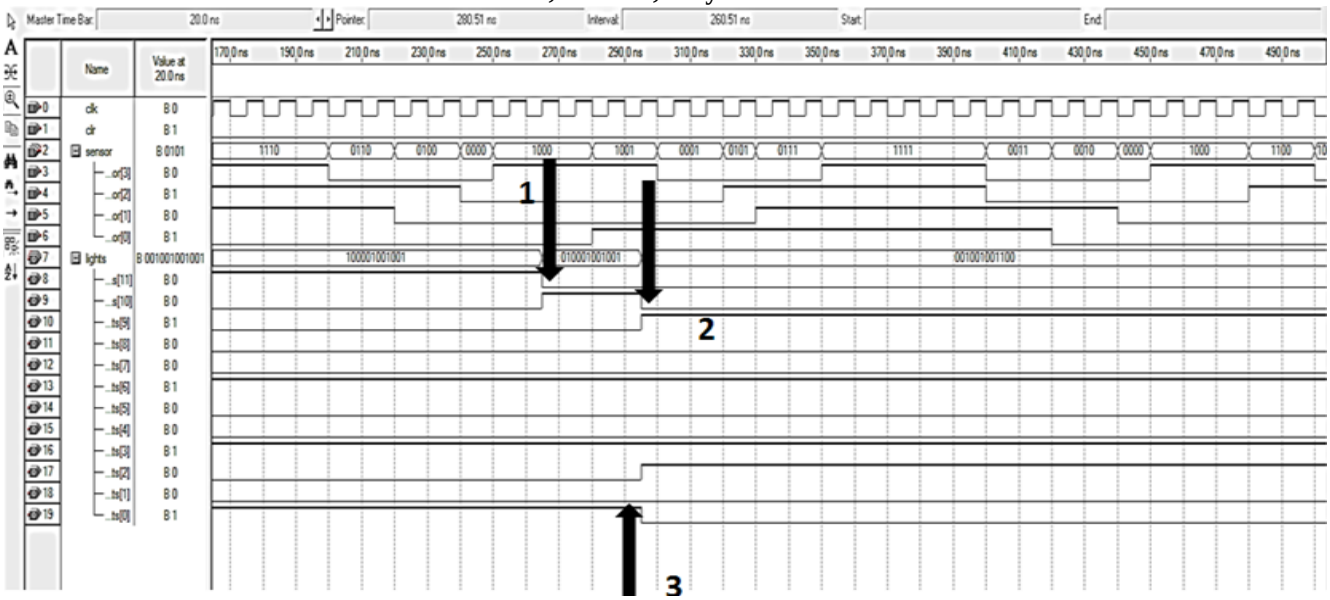

Fig 10: Simulation Behavioral Model When the North Traffic Light Changes From Green to Yellow

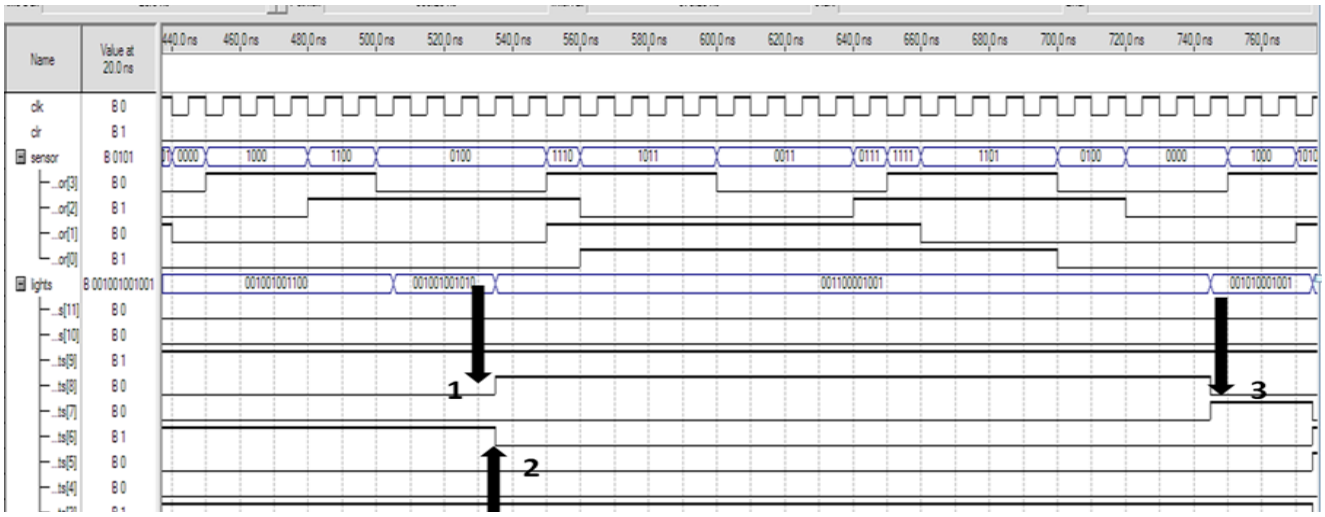

Fig 11: Simulation Behavioral Model when E_S is high

Table II: Description of I/O Bits

Sensor Bit	***Description***
Sensor[3]	North Sensor Input (N_S)
Sensor[2]	East Sensor Input (E_S)
Sensor[1]	South Sensor Input (S_S)
Sensor[0]	West Sensor Input (W_S)
Traffic Lights Bit	**Description**
Lights[11]	North green traffic signal
Lights[10]	North yellow traffic signal
Lights[9]	North red traffic signal
Lights[8]	East green traffic signal
Lights[7]	East yellow traffic signal
Lights[6]	East red traffic signal
Lights[5]	South green traffic signal
Lights[4]	South yellow traffic signal
Lights[3]	South red traffic signal
Lights[2]	West green traffic signal

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Lights[1]	Wet yellow traffic signal
Lights[0]	West red traffic signal

First thing that is obvious from fig 9, is the fact that no transitions occur when the clear (clr) input is high. This may also be referred to as the reset switch. When the clr signal is removed, only the green light for the North road is turned on (as shown by the arrow) due to a high input from N_S. Even though E_S and W_S are both high, the traffic signals at both the east and west roads are red due to the fact that the north has the highest priority as expected from the design. From fig 10, it can be seen that immediately after timeG, the green light goes off and then the yellow light for the north traffic comes on for a period given by timeY (shown by arrow 1), after which the red signal comes on(shown by arrow 2). Since sensor [0] or W_S is high at that point, the green signal for the west road comes on (arrow 3).

Fig 8 shows that the green and yellow signals for each traffic phase, last for the expected time periods. Since all sides share the same time period, we can show from the waveform that;

timeY= 1.015 µs – 985 ns = 0.03 µs and

timeG = 1.225 µs – 1.015 µs = 0.2 µs; are equal to the time periods set for the controller during the simulation.

Fig 11 shows the green traffic signal coming on for the East road when E_S is asserted (arrow 1). It should be noted that once the green traffic signal for a road is on, all other traffic lights will show the red signal. Arrows 1 and 2 simply show the change from red signal to green signal. The third arrow shows the yellow traffic signal coming on after timeG elapses.

III. CONCLUSION

In this paper, an FPGA based traffic light system capable of vehicle detection and real time control of traffic was developed. The design was divided into two main parts, with one part in control of the traffic state transitions, and the other in control of the length of time that each state would be asserted. Infrared sensors were used to send information to the FPGA regarding the presence or absence of vehicles in the form of discrete signals. The end result of the design, implementation, and debugging work is a controller implementation that has satisfied all aspects of the protocol described earlier, and has met all specifications necessary for a traffic light system, which is a giant leap in designing more complex systems. This system can be applied to any given set of intersecting roads with just slight adjustments to the VHDL code structure. Its use will aid in decongesting traffic along busy domestic and highway roads. Further research can be carried out on real time density control, to enable the intelligent traffic light system automatically switch to a more suitable traffic phase when it detects emergency vehicles of any kind (fire trucks, ambulances, police cars) on an oncoming lane.

Fig 12: Complete System Model

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