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Design of Process Variation 4-bit 50MS/s SAR ADC in submicron CMOS Technology

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Abstract*— This Paper presents the Design and Analysis of SAR ADC to develop process variation architectures. Data convertor ADC SAR architecture simulate on 1V, for 4 bit resolution .Design simulate for process variations with different submicron technology. Performance of convertor making it a promising choice for SAR ADC data convertor on chip structures for next-generation emerge digital systems. Process variation is mainly caused by fluctuations in dopant concentrate ions and device channel dimensions. Article contains logical design and simulation results of all design elements like comparator, DAC etc. Sampling frequency and power optimization can be further possible by enhancing the parameter of design as design test in as it form with minimum changes, not extensive optimization design trails. The performance of SAR ADC process variation is simulated in Cadence tool for effective performance for nanoscale technology alone with higher end tool Matlab shows it presence throughout soft computing calculation.

***Index Terms*— ADC, DAC, DNL, ENOB, INL, R2R, SAR, TSMC.**

I. INTRODUCTION

Successive Approximation ADC is often considered as one of the most popular A/D conversion techniques; because it offers the combination of high accuracy and low-power consumption. The SAR functionality can best be described as the implementation of a binary search algorithm. The block diagram of a Successive Approximation ADC is shown in Figure1 below. It consists of comparator, a DAC and Successive Approximation Register ADC (SAR). [4]

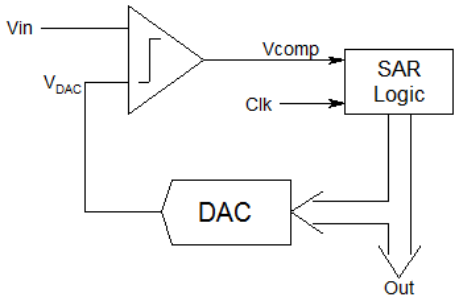

Fig 1-Principle of SAR-ADC

When an input signal is applied to the converter, the comparator simply determines whether the input signal is larger or smaller than the DAC output and produces one digital bit at a time starting from the MSB. The SAR stores the produced digital bit and uses the information to change the DAC output for the next comparison. This operation is repeated until all the bits in the DAC are decided. In order to achieve N-bit resolutions, Successive Approximation ADC requires N clock cycles. Because the performance is limited by DAC linearity, the calibration of the DAC is needed to achieve high resolution. Because the difference between input signal and reference successively gets smaller, circuit noise will limit the achievable resolution. Successive Approximation Register ADC represents the mainstream of the ADC market for medium to high resolution This topology requires just one comparator; an N-bit SAR ADC will require N comparison periods and will not be ready for the next conversion until the current one is complete. In contrast to the SAR, the average value of the difference between the input signal and reference remains constant making the algorithmic ADC less susceptible to comparator noise. However, a faulty decision will overdrive the input range to the following iterations, again with irreversible effect. The additional noise generated by the multiplication circuit, as well as the multiplication accuracy will limit the achievable resolution. Aside from the reduced hardware, the input capacitance of SAR ADC_S are often low, typically constraint by noise. [13]

II. COMPARATOR DESIGN

In order to precisely slice input data, a reference voltage may be transmitted, on a different signal path, along with the data. Alternatively, the data may be transmitted differentially. A differential amplifier input buffer amplifies the discrepancy linking the two inputs. In the simplest case one input to the input buffer is a DC voltage, say 0.5 V *(Vinm* in Fig.). When the other input *(Vinp)* goes above 0.5 V, the output of the buffer changes states (goes from a low to a high) or and

Vinp > *Vinm* -> out = “1”

Vinp < *Vinm* -> out = "0"

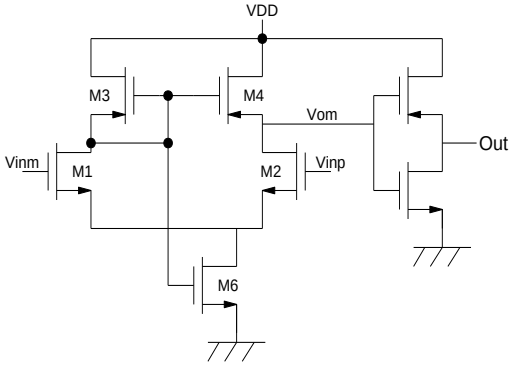

Fig 2- An input buffer for high-speed digital design

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The diff-amp in Fig1. is based on the topologies. This circuit is self-biased because no peripheral references are used to locate the current in the circuit. When *Vinp* is larger than *Vinm*, the current in M2 is larger than the current in Ml *(VGS2 > VGS1).* The current in Ml flows through M3 and is mirrored by M4 (and so M4's current is less than M2's current). This causes the diff-amp's output, *Vom,* to go towards ground (until the current in M2 equals the current in M4) and the output of the inverter, *Out,* to go high. Note that the gain from the *Vinp* input to the output of the circuit is larger than the gain from *Vinm* to the output (M3, being diode-connected, is a lower resistance than M4). It is generally a good idea to connect the reference voltage to the *Vinm* input. [1], [7], [9] an example transient response for the buffer in Fig1. is seen in Fig.3 below. A very small increase in *Vinp* above *Vinm* is required to make the output of the buffer switch states.

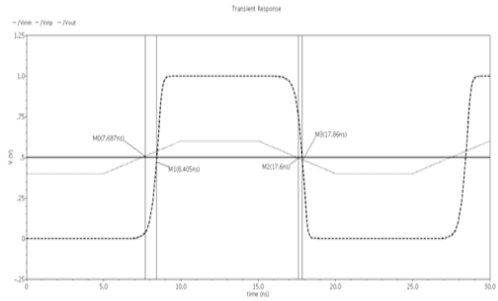

Fig 3- Transient response of the input buffer

Looking at Fig1, we can see that if the inputs fall below VTHN (threshold voltage NMOS), then the circuit won't work very quickly. So we would expect the propagation delays to increase. Ideally, the delay of the buffer is independent of power supply voltage, temperature, or input signal amplitudes. To get better performance for lower input level signals, we might use the PMOS version of the buffer in Fig. 1, as seen in Fig. 2. The delays are considerably better, however, there is an offset that appears rather large.

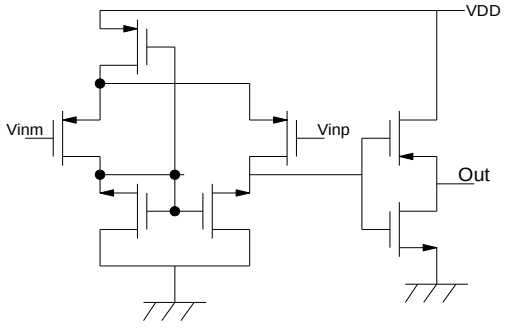

Fig 4- A PMOS input buffer for high-speed digital design

To avoid this offset, we might use the NMOS buffer in Fig. 1 with the PMOS buffer in Fig. 2 to form a buffer so as to operate well with input signals imminent ground or VDD. By using the buffers in parallel, the complementary nature results in a buffer that is robust and works over a ample range of operating voltages. We have designed four stage p-flavor and n-flavor input buffer to improve slew rate also. [6], [10], [11]

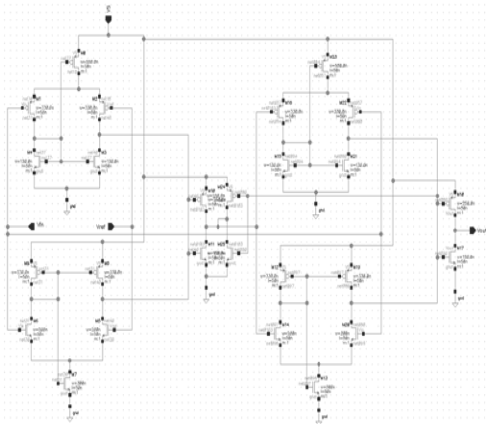

Fig 5- Practical design of comparator

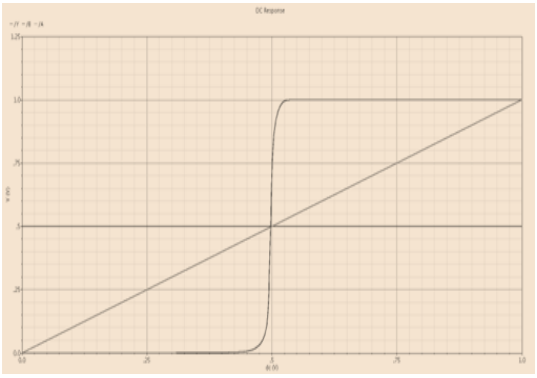

Fig 6- Output waveform of Comparator

Above Fig 6 shows the simulation result for two stage comparator of Fig 5 which shows the better performance of p-flavored and n-flavored in cascade form.

III. SAR LOGIC

The SAR logic for the ADC is a state machine which takes the Clock signal as input. The clock signal is divided by 8 to generate the clock. 6 clock cycles are required for one complete conversion. Two additional clock cycles are for Start of Conversion and End of Conversion.

i)The Start of Conversion (SOC) – 1st Clock cycle is used to reset all the registers in the logic block.

ii) The 2nd Clock cycle – Comparator performs comparison between Input data and reference voltage and generates a 1 or 0. The data is stored in the registers and applied to the DAC. The DAC sets the reference voltage for the next conversion cycle. The same process is repeated for 2nd to 7th clock cycle to complete conversion process.

iii) The End of Conversion (EOC) – 8th Clock cycle latches the output data to data bus.

The SAR logic operated over an 8 clock cycle period, with 2 cycles allotted for SOC & EOC and 6 clock cycles for digital data. [2], [3]

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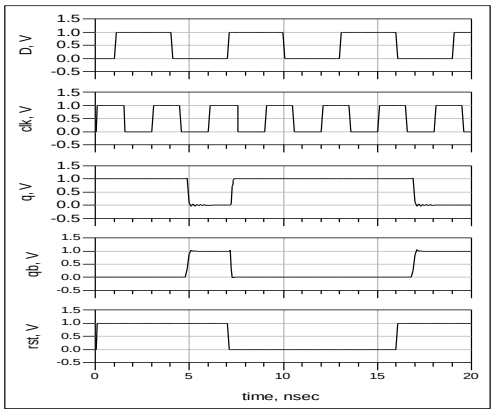

Fig 7- Output waveform of detdff

IV. R-2R DIGITAL TO ANALOG CONVERTER

One of the widespread DAC building-block structures is the R-2R resistor ladder network shown in Figure 8. It uses resistors of only two different values. An N-bit DAC requires 2N resistors, and they are relatively trimmed. There are also relatively few resistors to trim. The R-2R ladder consists of two different resistors placed in a configuration as shown in fig .The inputs to the ladder are fed from a N bit inputs. This configuration consists of a network of resistors alternating in value of R and 2R. Starting at the right end of the network, notice that the resistance looking to the right of any node to ground is 2R. Each node voltage is related to Vref, by a binary-weighted relationship caused by the voltage division of the ladder network. The total current flowing from Vref is constant, since the potential at the bottom of each switched resistor is always zero volts. Therefore, the node voltages will remain constant for any value of the digital input.

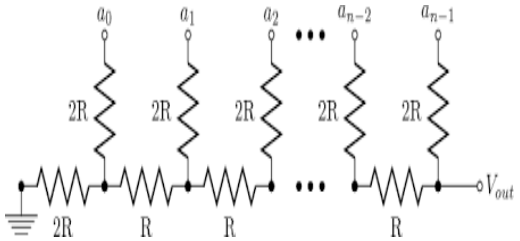

Fig 8- R-2R Ladder Network

It is not easy to construct a resistor-based DAC with a high resolution, due to the resistance spread, and the needs for 2N serial resistors. A better choice is the R-2R ladder this configuration consists of a network of resistors alternating in value of R and 2R. For a N bits DAC, N cells based on 2 resistors R and 2R are connected in serial. The digital input (d3, d2 d1 d0) determines whether each cell is switched to ground tied to Vdac through the resistors each cell's output voltage is a ratio of Vdac because of the voltage division of the ladder network. The final output voltage VOUT depends on the value of B, following the given formula equation (1).

$$V_{OUT}=V_{dac}\cdot\frac{(2^N-B)}{2^N} \quad \text{..... (1)}$$

On this principle, table I gives the value of VOUT versus the input code, with Vdac equal to 1V.

Table I- VOUT of 4 bit R-2R DAC verses input code

d3	d2	d1	d0	Vout
0	0	0	0	0
0	0	0	1	0.0625
0	0	1	0	0.1250
0	0	1	1	0.1875
0	1	0	0	0.2500
0	1	0	1	0.3125
0	1	1	0	0.3750
0	1	1	1	0.4375
1	0	0	0	0.5000
1	0	0	1	0.5625
1	0	1	0	0.6250
1	0	1	1	0.6875
1	1	0	0	0.7500
1	1	0	1	0.8125
1	1	1	0	0.8750
1	1	1	1	0.9375

a. INTEGRAL NON-LINEARITY (INL)

Due to the non-ideal behavior of switches, process fluctuations and various gradient effects, there exist a small difference between the ideal analog output "Vout_ideal" and the actual analog output "Vout". The deviation of "Vout"from the ideal value "Vout_ideal" is called the integral non-linearity (INL).The normalized integral non-linearity can be given by equation (2). An example of transient response for the buffer in Fig.1 is seen in Fig.3 below. A very small increase in *Vinp* above *Vinm* is required to make the output of the buffer switch states.

$$INL_i=\frac{Vout_i-Vout_{ideal}}{\Delta V} \quad \text{..... (2)}$$

b. DIFFERENTIAL NON-LINEARITY (DNL)

The difference between two adjacent analog outputs may be significantly different from the theoretical voltage step. This deviation is called the differential non-linearity (DNL). The normalized differential non-linearity includes the voltage step ΔV to get the relative error. Figure illustrates the difference between INL and DNL concepts. [5]

$$DNL_i=\frac{Vout_{i+1}-Vout_i-\Delta V}{\Delta V} \quad \text{..... (3)}$$

The SAR ADC performed with an average of 0.0074 LSB differential nonlinearity (DNL) and a mean integral nonlinearity (INL) of 0.0137 LSB. Figs.10 and 11 show plots of measured DNL and INL, respectively, as a function of the output digital code. [8], [12], [13]

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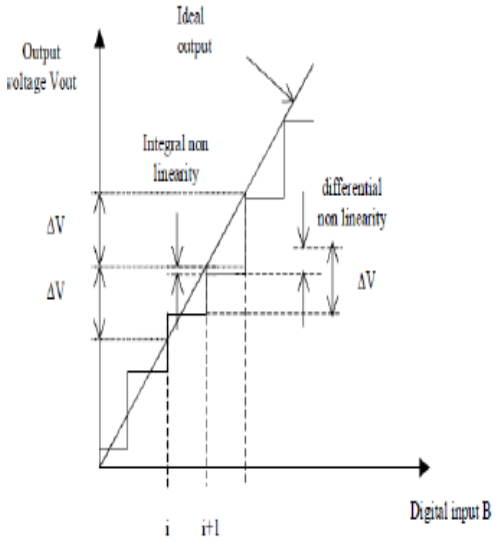


Fig 9- The intend of integral and differential non-linearity

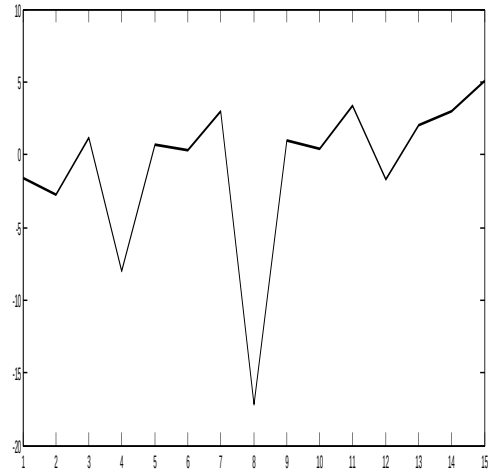


Fig 10- Plot for DNL

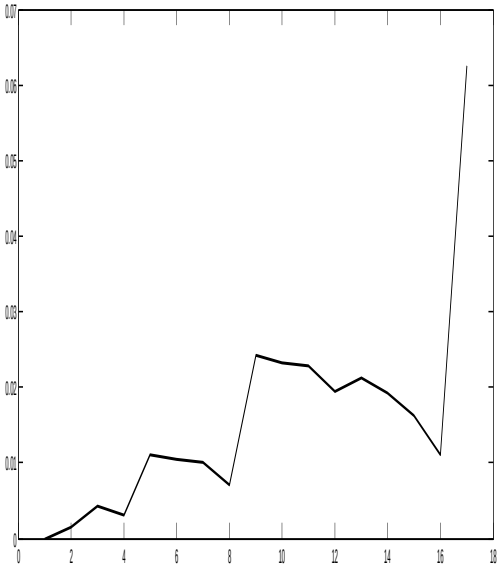


Fig 11- Plot for INL

Table II-Readings of R-2R DAC circuit

Digital Inputs				Analog o/p Value		INL	DNL
d3	d2	d1	d0	Ideal o/p voltage (V)	Actual o/p voltage (mv)		
0	0	0	0	0	0	0	0
0	0	0	1	0.0625	65.5	0.0016	-1.580
0	0	1	0	0.1250	125	0.0043	-2.720
0	0	1	1	0.1875	187	0.0031	1.200
0	1	0	0	0.2500	250	0.0111	-8.000
0	1	0	1	0.3125	312	0.0104	0.700
0	1	1	0	0.3750	375	0.0101	0.300
0	1	1	1	0.4375	437	0.0071	3.000
1	0	0	0	0.5000	500	0.0243	-17.20
1	0	0	1	0.5625	562	0.0233	1.00
1	0	1	0	0.6250	625	0.0229	0.400
1	0	1	1	0.6875	687	0.0195	3.400
1	1	0	0	0.7500	750	0.0212	-1.70
1	1	0	1	0.8125	812	0.0192	2.00
1	1	1	0	0.8750	875	0.0162	3.00
1	1	1	1	0.9375	937	0.0111	5.10

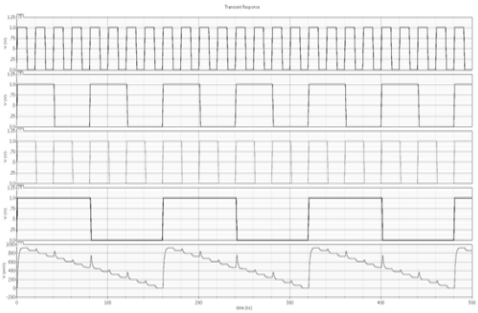
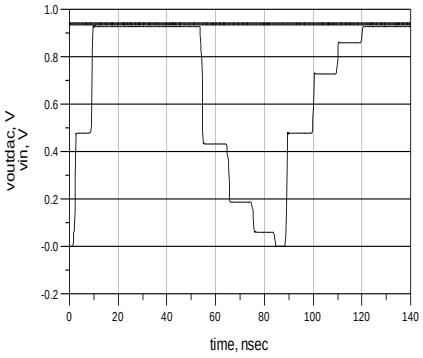


Fig 12- r2rdac output waveform

Fig 12 shows the corresponding transient analysis waveform for r2r dac.

V. SIMULATION RESULTS OF ADC

Figure 13 (a) and (b) shows the simulation result for 4-bit SAR. Fig (a) gives the evaluation of dac output and applied input voltage. Whereas Fig(b)shows waveform for corresponding dac input code.



(a)

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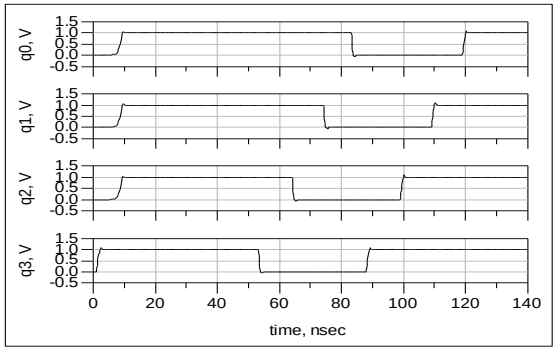

(b)

Fig 13- (a) and (b) SAR output waveform

Table III - Performance summary of proposed ADC

Mode	Obtained Value @ 0.18µm	Obtained Value @ 50nm
Supply Voltage	1V	1V
Sampling freq.	22.72MHz	50Mhz
Power	1.095mW	166µW
Resolution	4-bit	4bit
Technology	0.18µm	50nm
INL	0.0137 LSB	~0.0137 LSB
DNL	0.0074 LSB	~0.0074 LSB
SNR_{db}	25.84db	~25.84db
ENOB	4	4

VI. CONCLUSION

This paper presents the design and analysis of 1 V 4-bit SAR ADC in 0.18µm and 50nm having very low power consumption high sampling frequency. The Process variation design of ADC is investigated and SAR architecture is chosen of 4 bit resolution designed and analyzed. Transient and parametric analyses were carried out in the simulation process. Process variation is simulated in cadence for effective performance for Nanoscale technology. Thus it can be used for on chip data convertor in emerge digital systems, embedded microprocessors, as well as for stand-alone ADCs. From the above results of Power calculation of SAR ADC of the different technologies it is observed that power consumption decreases as technology uses increases.

VII. ACKNOWLEDGMENT

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