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Design and Implementation of FFT/IFFT System Using Embedded Design Techniques

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Abstract*—The paper proposes a design of soft core processor system accommodated to perform Fast Fourier Transform and Inverse Fast Fourier Transform (FFT/IFFT) of a discrete input signal. A DDR SDRAM 64M byte memory is introduced to the system to cope with high density storage requirements of high frequency signals. Xilinx Microprocessor Debugger (XMD) is used to initialize the DDR SDRAM with the C-language program that is used to perform the signal transform. The system is designed using ISE tool software and configured on Spartan-3E FPGA Slice.

***Keywords*—DDR SDRAM, Embedded design techniques, Spartan-3E FPGA Slice, and XMD debugger.**

I. INTRODUCTION

An embedded system is designed to continuously execute a specific set of tasks for a particular application. In general, embedded systems have a hardware component and a software component designed to be executed on the hardware. The hardware component consists of a microprocessor and associated peripherals. Embedded systems can be utilized in a wide variety of applications, ranging from consumer electronics to industrial equipment.

FPGAs serve as a real-time prototyping and implementation medium on which complete embedded systems can be implemented to test and verify their functionality. This has encouraged embedded systems designers to increasingly use FPGAs as their implementation medium in order to minimize design costs and time [1].

In [2], Sheac *et al.* presented two FFT implementation approaches, one implementation as an FPGA co-processor and the other using only an external digital signal processor.

In [3], Mounir Arioua *et al.* presented an optimized implementation of the 8- point FFT processor with radix-2 algorithm in R2MDC architecture. The butterfly- Processing Element (PE) used in the 8-FFT processor reduces the multiplicative complexity by using a real constant multiplication in one method and eliminates the multiplicative complexity by using add and shift operations in other proposed method.

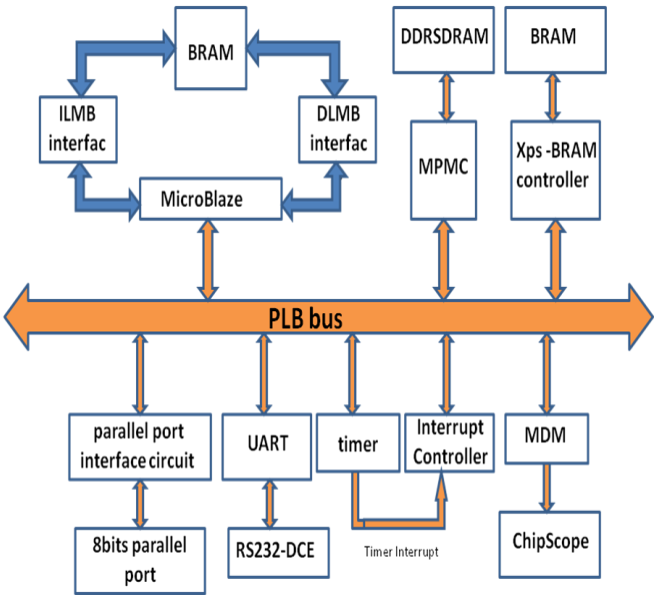
The paper is organized to include constructing a soft core Processor system using embedded design techniques, theoretical review of FFT, IFFT calculation, and developing a C program oriented algorithm for calculating FFT/IFFT. Results are displayed using chip scope window and discussed. Finally conclusions are introduced.

II. CONSTRUCTION OF A SOFT CORE PROCESSOR SYSTEM

Embedded Design Kit tools (EDTs) [4] are used to develop the soft core processor system that implies micro blaze soft core processor [5]. Processor Local Bus (v 4.6) [6] to transfer data, addresses, and controls signals. 16 K byte block RAM [7] to act as boot memory with instruction local memory bus (ILMB) and data local memory bus (DLMB) [8], interrupt controller, debug module to be connected with chipscope window to display selected captured signals and DDR SDRAM connected to PLB via MPMC interface.

The system requires an I/O port to be used for data acquisition therefore 8 bits parallel I/O port is designed and added to the system using CIP with the techniques adopted in [9].

The hardware part of the designed system with its address map is shown in Fig 1. The designed processor system is programmed using C- language and adapted to calculate the FFT/IFFT of a discrete signal.



(a)

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Instance	Name	Base Address	High Address	Size	Bus Interface(s)	Bus Connection
dlmb_cntlr	C_BASEADDR	0x00000000	0x00001fff	8K	SLMB	dlmb
ilmb_cntlr	C_BASEADDR	0x00000000	0x00001fff	8K	SLMB	ilmb
debug_module	C_BASEADDR	0x84400000	0x8440ffff	64K	SPLB	mb_plb
xps_bram_if_cntlr_1	C_BASEADDR	0x85200000	0x85209fff	8K	SPLB	mb_plb
xps_intc_0	C_BASEADDR	0x81800000	0x8180ffff	64K	SPLB	mb_plb
xps_timer_1	C_BASEADDR	0x83c00000	0x83c0ffff	64K	SPLB	mb_plb
RS232_DTE	C_BASEADDR	0x84000000	0x8400ffff	64K	SPLB	mb_plb
RS232_DCE	C_BASEADDR	0x84020000	0x8402ffff	64K	SPLB	mb_plb
DDR_SDRAM	C_MPMC_BASEADDR	0x86000000	0x87ffffff	32M	SPLB0	mb_plb

(b)

Fig 1. The designed embedded processor system
(a) . The block diagram of the hardware part
(b) . The address map

III. FAST FOURIER TRANSFORM

The Fast Fourier Transform is an optimized computational algorithm to implement the Discreet Fourier Transform of an array of N samples. It allows determining the frequency contents of a discreet signal, representing the signal in the frequency domain.

The algorithm of Cooley-Tukey is used in this work to perform FFT. The FFT is calculated in two stages, the first stage transforms the original data array into a bit-reverse order array by applying the bit-reversal method, and the second stage processes the FFT in $N*\log_2(N)$ operations (by applying Danielson-Lanczos Lemma algorithm) [10] [11].
FFT calculation is based on the DFT equation:

$$F(n) = \sum_{k=0}^{n} x(k)\, W_N^n \qquad \text{---------- (1)}$$

Where
n= 0, 1… N-1 , N: number of samples , x (k): input signal

$$W_N^n = e^{-\frac{j2kn\pi}{N}} \qquad \text{---------- (2)}$$

W_N^n is known as twiddle factor.

Equation (1) can be broken up in two summations of half the size of the original. The summation is the "even terms", E, and the second is the "odd terms", O, as shown in equation (3):

$$X(n) = \sum_{k=0}^{\frac{N}{2}-1} x(2k)e^{-\frac{j2kn\pi}{(\frac{N}{2})}} + W_N^n \sum_{k=0}^{\frac{N}{2}-1} x(2k+1)e^{-\frac{j2kn\pi}{(\frac{N}{2})}} \qquad \text{------- (3)}$$

E=Even Term (N/2 Point DFT of even indexed sequence)
O=Odd Term (N/2point DFT of odd indexed sequence)

The first step to perform FFT is to break the transform into the two (N/2)-point transforms and the W_N^n provides the N-point combining algebra.
Each of the (N/2)-point sequences can be decimated further into two sequences of lengths N/4, each (N/4)-point transform is broken into two (N/8)-point DFTs, as shown in Fig 2. This process can be continued until there are $\log_2$ N stages it is listed is in the following patterns.

Input Order		*Binary*		*Reversed*		*Output Order*
0	→	000	→	000	→	0
1	→	001	→	100	→	4
2	→	010	→	010	→	2
3	→	011	→	110	→	6
4	→	100	→	001	→	1
5	→	101	→	101	→	5
6	→	110	→	011	→	3
7	→	111	→	111	→	7

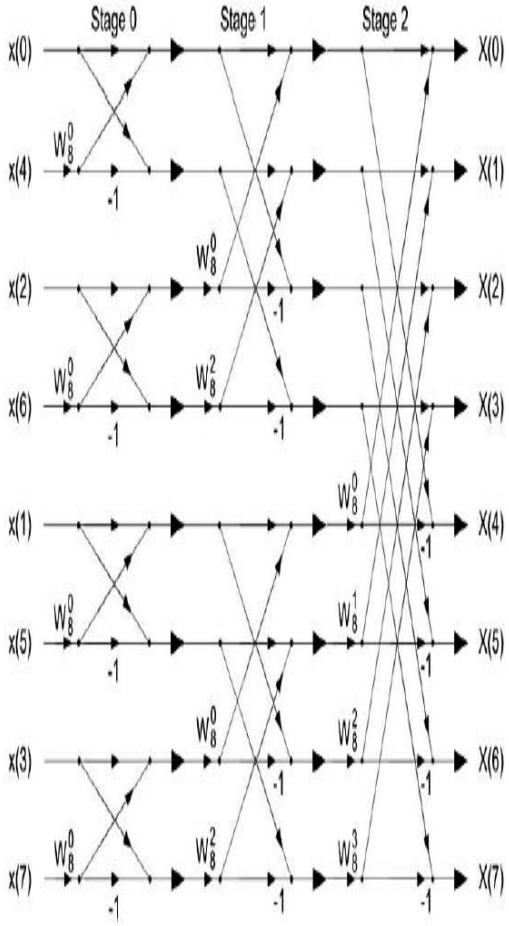

Fig 2. The flow graph for an eight-point decimation-in-frequency Fast Fourier Transform algorithm

The flow chart of the prepared program is shown in Fig 3.

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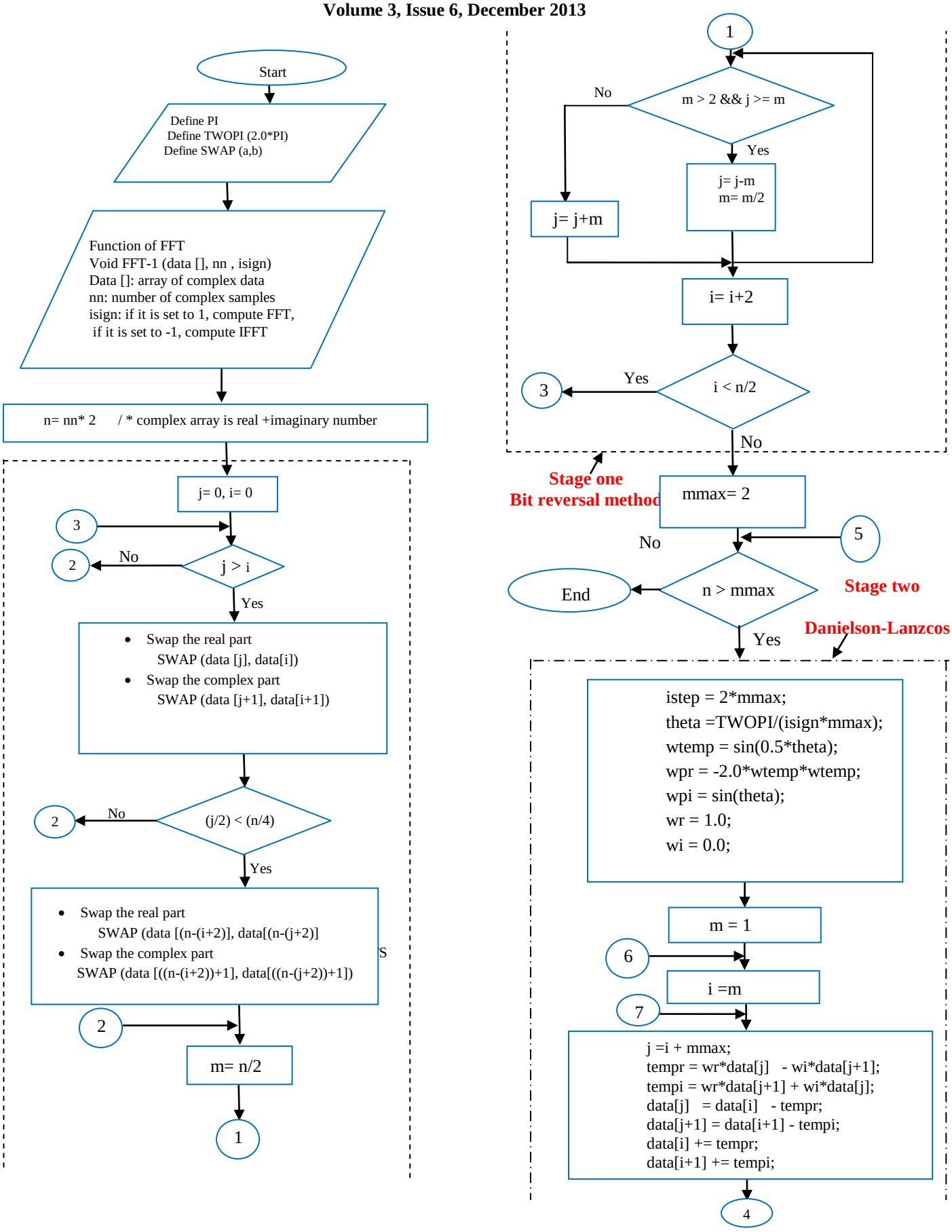

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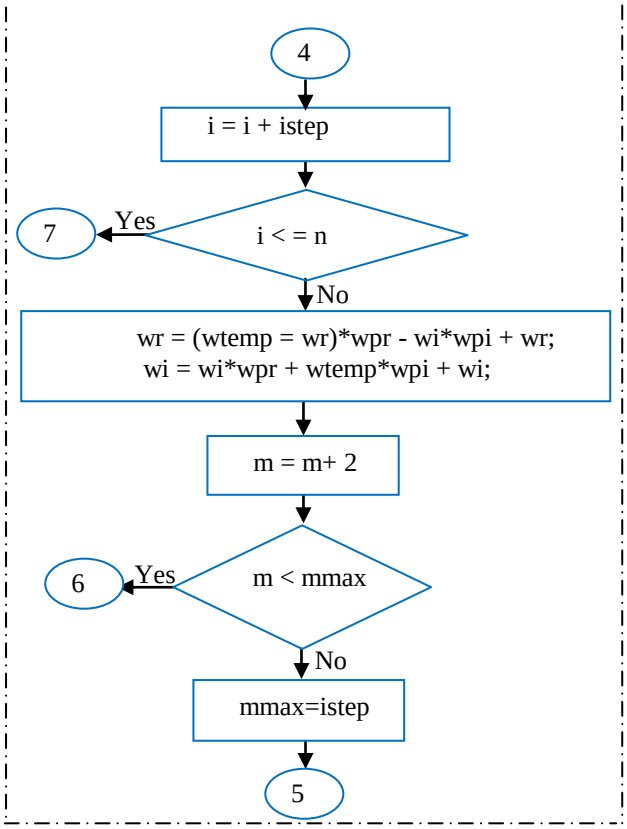
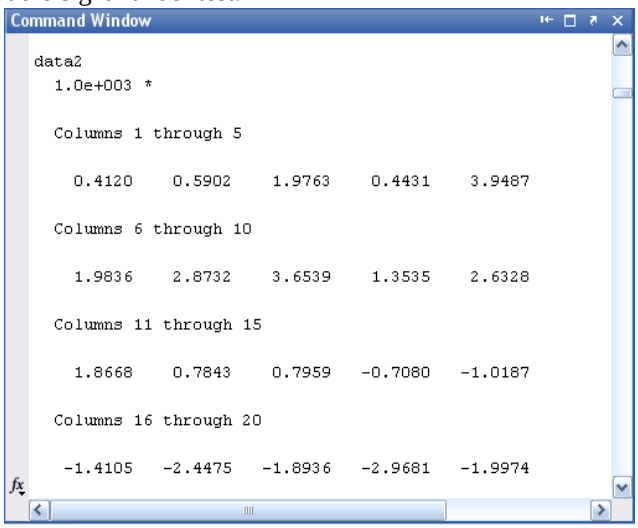


Fig 3. The FFT/IFFT flow chart algorithm

IV. RESULTS

An audio signal is introduced to the designed system via the added parallel port to be processed where its FFT and IFFT are calculated. The audio signal under test is generated in matlab media and transmitted to the designed processor system. Fig 4 shows the first and last twenty samples of the audio signal under test.



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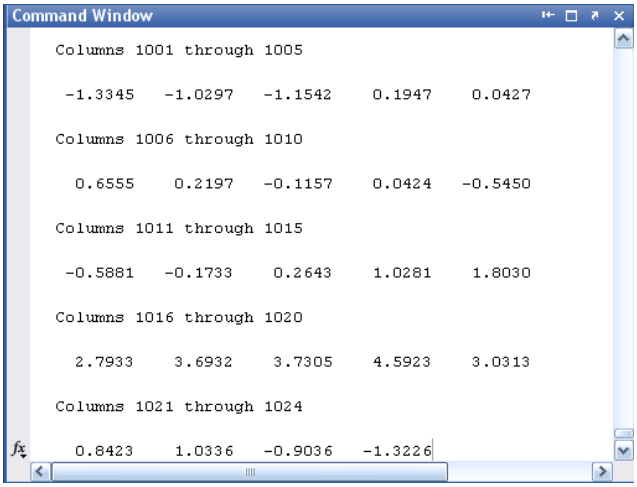

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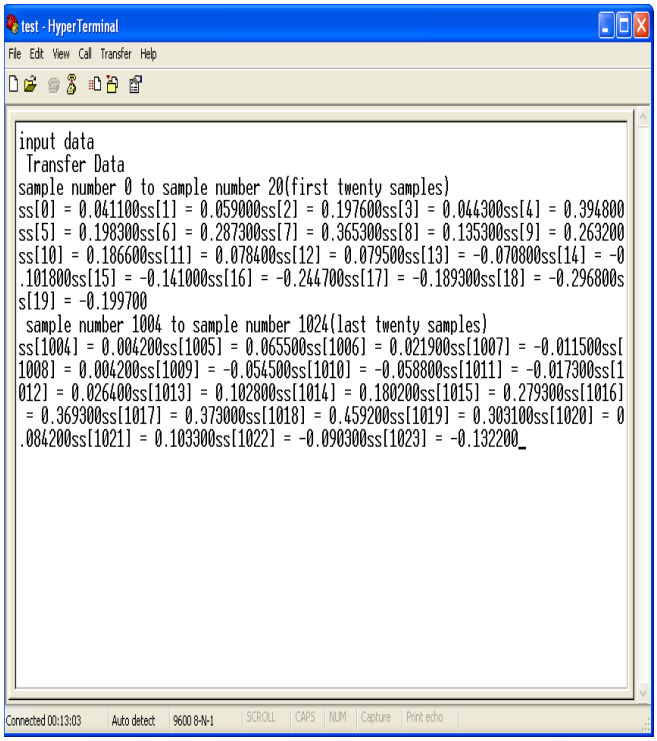

(c)

Fig 4. The first and last twenty samples of the test signal

(a). First twenty samples in matlab media
(b). Last twenty samples in matlab media
(c). First and last twenty samples in the FPGA media displayed on hyper terminal window

Fig 5 shows the samples of the acquired signal displayed on chipscope window.

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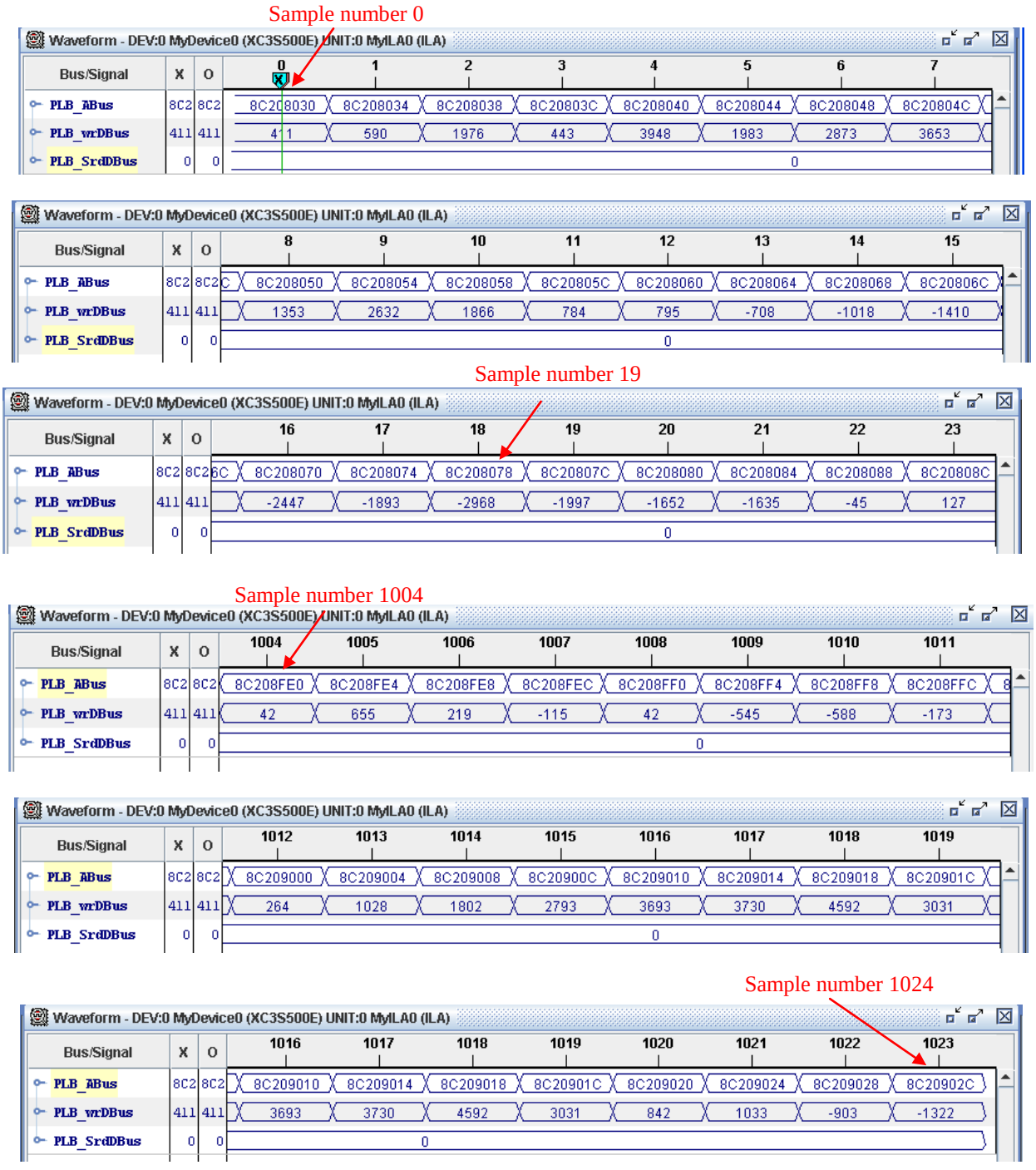

Fig 5. Samples of the data received by the processor system via the designed port displayed on ChipScope window

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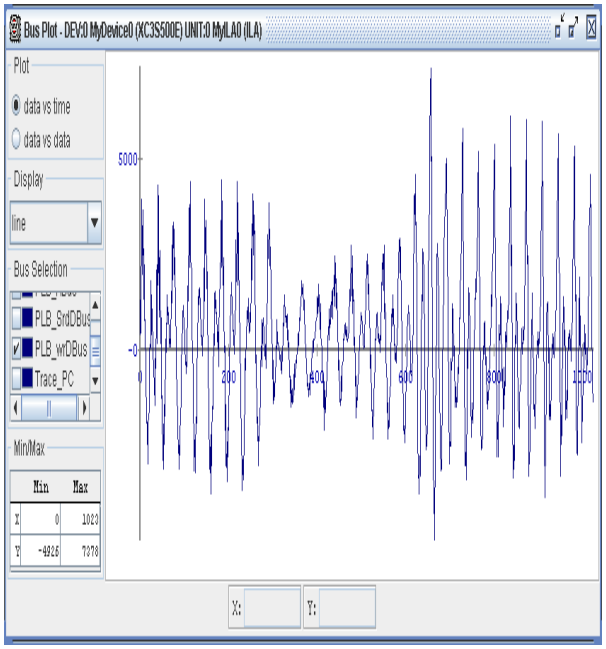
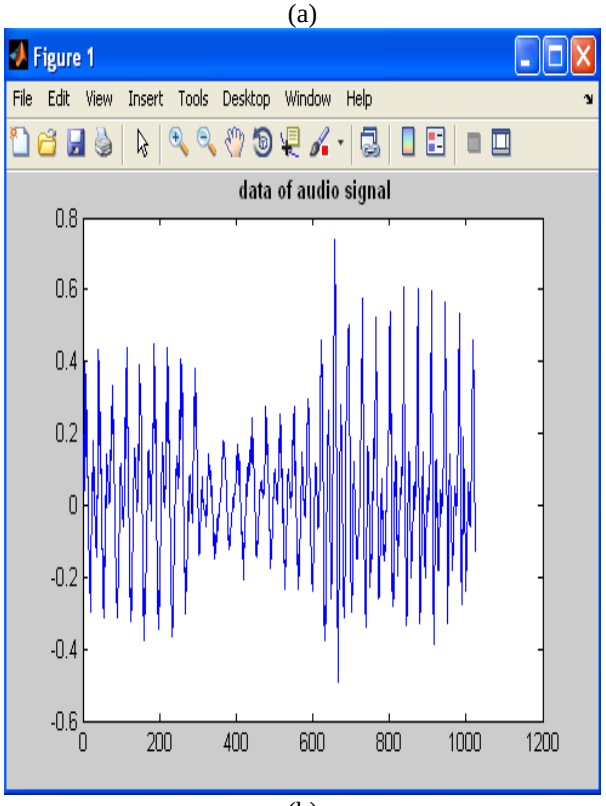
Fig 6 shows the test signal with its Fast Fourier Transform processed at each 64 samples in embedded processor system media displayed on chipscope and compared with the results obtained by matlab.



(a)



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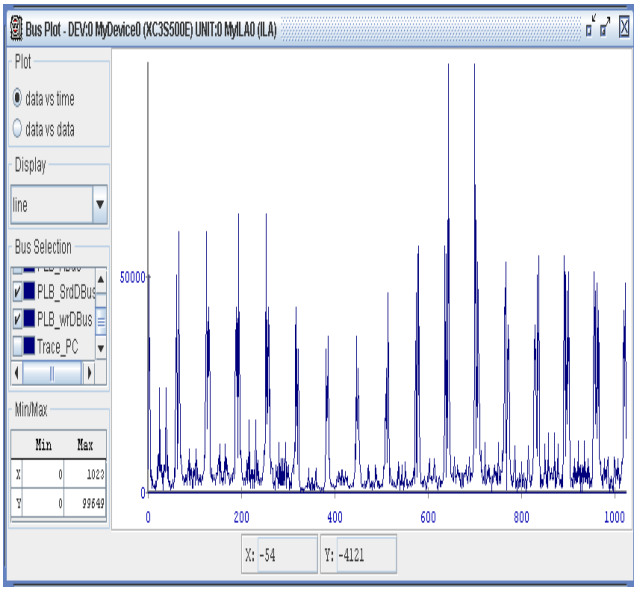

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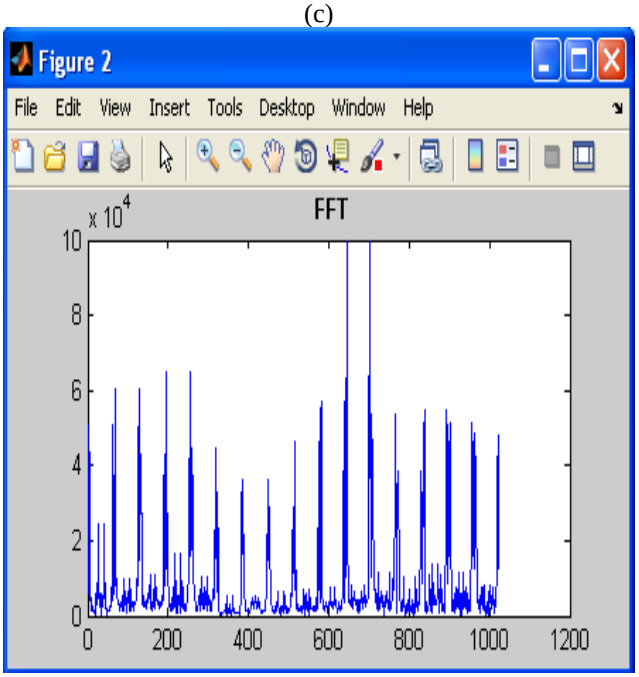

(d)

Fig 6. Fast Fourier Transform of the test signal
(a) . Test audio signal displayed on ChipScope window
(b) . Test signal in matlab media
(c) . FFT of the test signal performed by the designed system shown in chipscope window
(d) . FFT of the test signal calculated in matlab media

Fig 7 shows the IFFT of the signal computed each 64 samples transformed by the designed system and compared with matlab results.

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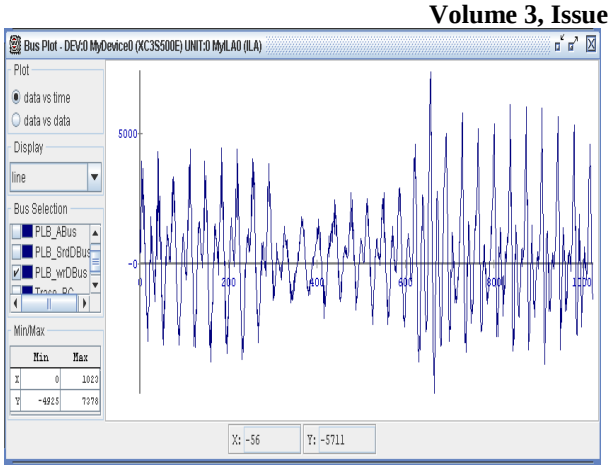
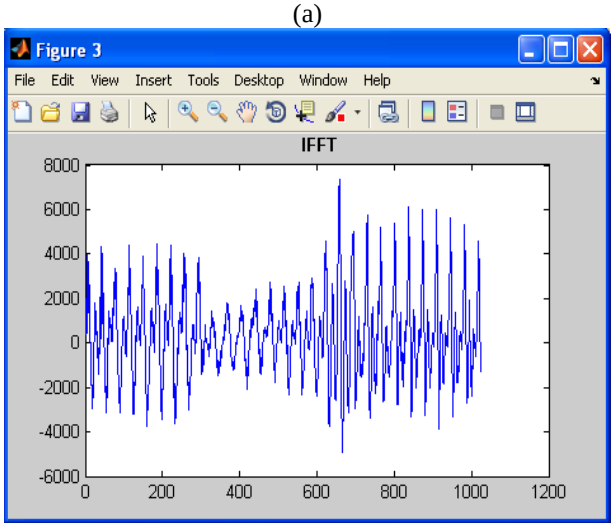


(a)



(b)

Fig 7. Inverse Fast Fourier Transform of the received signal computed for each of the 64 samples
(a). IFFT computation of test signal in embedded processor media displayed on ChipScope window
(b). Computation results shown on matlab media plotter

V. CONCLUSION

An embedded processor system is designed and configured on Spartan 3-E Slice. The system is accommodated to compute the FFT of any signal and it's IFFT. The computation could be performed for any number of samples by setting the interrupt controller to acquire the signal at certain predefined interval. The system is able to deal with high frequency contents signals as image signals as it include a 64 M byte DDR SDRAM.

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AUTHOR BIOGRAPHY

Mazin R. Khalil assistant professor in Technical College of Mosul. He published 32 papers in Electronic and Computer fields. He supervised 18 M.S.C students. His research interests are in implementation of FPGA and embedded system.

Aseel Thamer Ibrahem was born on 10 th Jan 1983. She received the B.E degree in Computer Technology Engineering from Technical College of Mosul, Iraq in 2004. She is working in Technical College of Mosul. Her research interests are in implementation of signal processing functions and wired communication systems on FPGA.