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Address Remapping in Arithmetic Functions using ROM Based Approximation Approaches

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Abstract*— in the piecewise function evaluation a non-uniform segmentation method for arithmetic function is evaluated based on polynomial approximations. Function evaluator is very much dominant task in the field of VLSI. Entire system speed or performance depends on how fast functions are calculated and solved. Few works already has been done based on uniform segmentation and non-remapping of ROMs. In my work trigonometric and logarithmic functions are considered. To evaluate functions ROM plays a major role in terms of accessing. Faster the ROM accessing faster the evaluation of functions. However to evaluate the functions the speed of the adders and multipliers also plays key effect on parameter speed and time. This work follows two approaches to make a evaluation faster. One is ROM address remapping with non-uniform segmentation. Second is replacing faster adders and multipliers. Speed/time, power are the two important parameters which will define this better. I propose a new non uniform segmentation method that searches for the optimal segmentation scheme with the goal of minimized ROM, total area.

***Index Terms*—function evaluation, non-uniform segmentation, polynomial approximation, ROM.**

I. INTRODUCTION

The function evaluation is often performed by many compute-bound applications. Elementary functions and compound functions are examples of these functions. Software implementations are too slow for real-time applications. Hence it depends on hardware function evaluators to perform these applications. Arithmetic function calculation is done based on table-based method. The table-based method is divided into two categories namely piecewise table lookup method and bipartite/multipartite table method. These methods differ in their on-the-fly computation circuits. Piecewise table lookup method contains adders, multipliers and ROM whereas multipartite table method contains only ROMs and adders but no multipliers. The main objective of piecewise method is to cut the input range into shorter intervals so that approximated formula can be applied with few terms to achieve target accuracy at each interval. Numerical functions such as exponential, logarithmic, trigonometric are widely used in many applications such as communications, computer graphics and digital signal processing. Hardware implementations of function evaluators have been developed to speed up these function approximations.

II. FUNCTION EVALUATORS

In general there are three categories of hardware function evaluators namely table-bound, compute-bound, and in-between. The innovation of my work include a method of polynomial approximations with nonuniform segmentation, hardware architecture and implementation, and evaluation of this implementation with a trigonometric and logarithmic functions. The methods of designing function evaluation is based on three methods namely address remapping, non-uniform segmentation, and FPGA implementation. Memory of addresses are taken into account by which it is mapped using ROM. Polynomial approximations are considered and those expressions are given to the memory. Lookup table stores these memories and is evaluated for the given approximate functions. Address remapping maps the addresses of the function evaluators and hence it reduces the size of ROM by reducing the memories in the lookup table. Hierarchical segmentation partition the interval of functions in adaptive manner and produces polynomial coefficients. Hardware generation utilizes the segmentation and coefficients and produces VHDL code which is suitable for ASIC or FPGA implementation. The input is given to least significant bit and most significant bit by which address is calculated and segmented within the intervals. ROM output is given for scaling the final result. The scaling circuit involves shifters which increases or decreases the values. Function evaluator calculates the segments and remaps the addresses to scale the ROM which signifies the scaling operation of the function evaluated. Thus remapping is essential factor in function evaluators. Hence function evaluators play a vital role in address remapping and non-uniform segmentation.

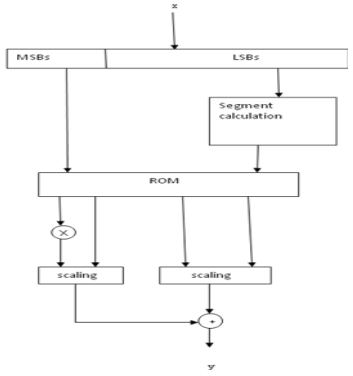

Fig 1: Function Evaluation Architecture

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III. SEGMENTATION AND REMAPPING

The segmentation is divided into two categories namely uniform segmentation and non uniform segmentation. The aim of uniform segmentation is to divide inputs into uniform segments of equal length to achieve a piecewise polynomial segments. A non uniform segmentation merges a fixed number of uniform segments into a large segment. The major drawback of non uniform segmentation is additional hardware cost and delay to access polynomial coefficient ROM.

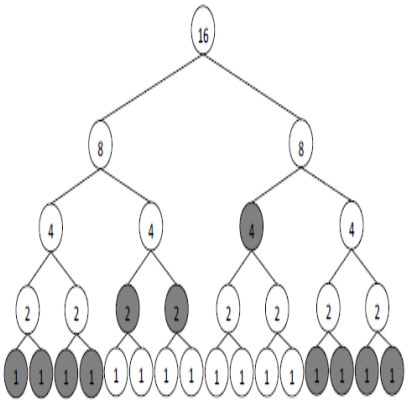

Fig 2: decision tree of non uniform segmentation

Figure 2 shows an example of determining non uniform segmentation for the 16 uniform segments. Each gray circle denotes the non uniform segments while the number inside it indicates the count of merged segments inside it. Optimal polynomials are used to decrease the degree of polynomial chosen as much as possible. That is the goal is to minimize the approximation error from the polynomial approximations. Chebyshev and minimax methods are used in uniform segmentation whereas in non uniform segmentation remapping and hierarchical transformations are used. Two degrees of polynomials are used to determine the sum of degrees of the factors. Degree 1 polynomial gives linear approximation technique and degree 2 polynomial gives quadratic approximation technique. Address remapping will eliminate the adder required in the address generation. New start address can be rearranged by replacing the least significant bits with bit patterns. After remapping new address is formed which reduces ROM size. The algorithm used is of four major subroutines namely uniform, non uniform, grouping, remapping. Address generator will generate the address to the main memory and process is done in the processing unit.

IV. SIMULATION AND RESULT ANALYSIS

In order to reduce the size of ROM address remapping is used to simulate the function. VHDL is used to synthesis the generation. Hence trigonometric and logarithmic functions are generated for fast accessing of ROM. The clock pulse is given and reset the address. Samples of addresses are taken and output memory addresses are generated. Such that it reduces the memory address space occupied.

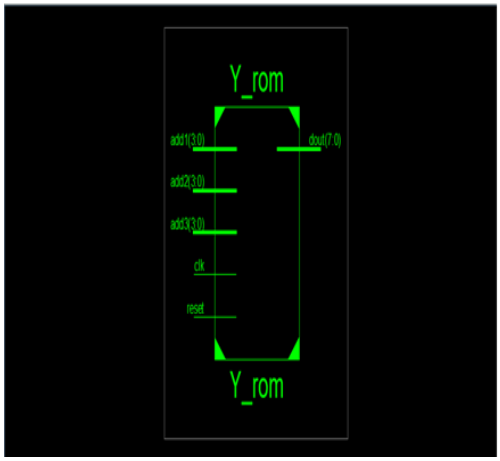

Fig 3: RTL schematic of ROM

The RTL schematic shows that the address is given from 0 to 3 and the data lines are from 0 to 7. So that it generate sequence of address to the ROM. The simulation result is given below which describes the address generated in the ROM. The memory addresses are simulated in the figure 4 as shown below. Thus the size of memory stored in ROM is reduced.

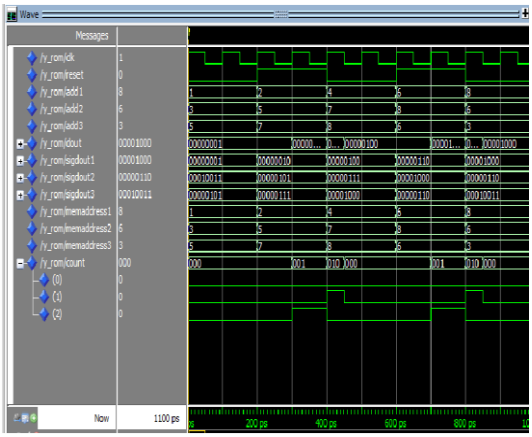

Fig 4: Simulator result of ROM

V. CONCLUSION

This paper develops basic idea of reducing memory of function evaluators using ROM. Thus by reducing memory speed of the operation can be increased and delay is reduced.

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