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Diode Based Ground Bounce Reduction for 3 bit-Fat-Tree Encoder in Analog to Digital Converter

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Abstract*— Analog-to-Digital converter is a useful component in the signal processing and communication system. Challenges that the designing of high speed devices and converters in the digital signal processing is facing are low power and low voltage. . Flash ADC is required the efficient design and reduced complexity for high speed and low power devices in signal processing system. This paper describes the ultra high speed ADC design with a fat tree encoder that became highly suitable and accurate. Speed becomes the important part that enhanced by component of 2 guidelines of fat tree encoder. A 3 bit ADC has been designed and simulated in CMOS 45 nm technology with input voltage range of 0 V to 0.7 V. The simulated and analyzed results show low power and a high speed performance for optimised ADC. This paper reports the power gating technique to provide reduction mechanism for suppressing the leakage current effectively during standby mode but it introduce ground noise. We designed a "3" bit flash ADC with power gating technique to reduce leakage current and ground bounce noise in different mode.. This diode based power gating technique provides reduction of leakage current in standby mode, and reduction of ground bounce noise in sleep-to-active mode. The improved power gating technique provides 82% reduction in leakage current, and 73% reduction in ground bounce noise as compared with conventional flash ADC. Fat-tree Encoder with diode based stacking power gating technique has been designed with the help of cadence tool at various supply voltages with 45 nm technology.

***Index Terms*—Active power, Diode based stacking power gating, Fat-tree Encoder, Flash ADC, Ground bounce noise, Leakage current.**

I. INTRODUCTION

ADC stands for Analog-to-Digital converter. Analog to Digital converter is a more useful component which helps to make up blocks in today's electronic system. ADC is a system which has a high speed operation it is designed as a faster component. ADC is the required 2n – 1 comparator for a n-bit A/D converter [1]. ADC has been used in every consumer electronics and computer systems. When we need high speed and low power application, we use flash ADC [2]–[5]. In recent years, system on chip grows rapidly. Analog to digital converter (ADC) is a mixed signal integrated component that converts analog signals to digital signal; which are real world signals to digital signals for information processing component. Analog to digital converter demand increasing rapidly because digital inverter has Design of high speed, low operating voltage, low power consumption and high input signal bandwidth [6]-[10]. Comparator is the important component of any flash ADC and its performance are comparators because ADC depends on comparators. Area, speed and power consumption of computational intensive VLSI systems are contributed and well implemented by flash ADC. Low power and high speed flash ADC are in high demand [11]. Technology is making size of device is smaller, so it has become difficult to achieve a good tradeoffs by device scaling or sizing the transistors [12]. Gate leakage increases 30 times with new technology [13]. To reduce the leakage improved design techniques are important. Sleep transistor is connected between the actual ground and circuit ground in the power gating technique [13]-[14]. To cut the leakage path the sleep mode of this transistor was off. Power gating technique reduces the leakage with minimal impact on the performance of circuit [15] Other power gating techniques are Multi-threshold CMOS (MT CMOS) [16] and Transistor Gating [17].These all reduce leakage current and ground bounce noise. Focus of this paper is reducing sub-threshold leakage power and ground bounce noise, with the help of a diode based stacking power gating technique.

II. PROPOSED DESIGN AND TECHNIQUES

A. Flash ADC

Figure (1) show block diagram of conventional flash ADC which is implemented using cadence virtuoso tool with 45 nm technology .Typical 3 bit flash converter is implemented here. Flash"3" bit converter, simply require 23-1= 7 comparators. A resistive divider that incorporated in converter employ 23 = 8 resistors require for providing the reference voltage to comparators.

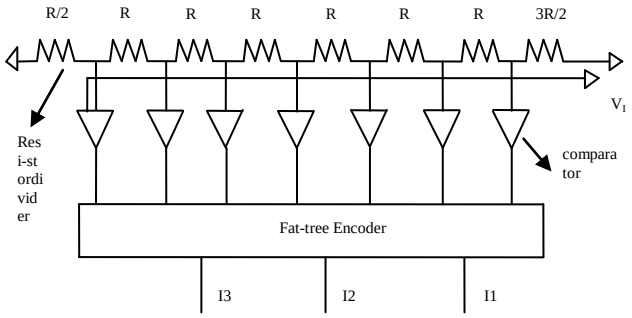

Fig 1. Conventional flash ADC architecture [18]

The reference voltage provided by resistive divider to each comparator is one LSB (least significant bit) that is higher than the reference voltage for the comparator just below it.

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Each and every comparator achieved the output "1" whenever input voltage source (analog) Vin is higher than the reference voltage Vref provided to comparators .The comparator give output "0"when analog input source is lower than reference voltage applied to it. Each resistor in divider section divides the reference voltage that is applied in upper extreme resistor to feed a comparator. Each and every comparator achieved the output "1" whenever input voltage source (analog) Vin is higher than the reference voltage Vref provided to comparators. . The output of the comparators is not in digital form but it is to be encoded. Therefore a Fat-tree encoder is employed to convert the encoded signal into digital form means "n" bit data format that is binary code. Higher the resistance value, the lesser is the current consumed by the device. This contributes to the minimization of power dissipation in the device .Flash ADC "n" bit architecture provide 2n-1 comparators that consist of differential amplifier based. ADC can operate at speed higher and will consume less power, it can operate easily. In designing the high speed ADCs, the code converter plays an important role in speed of and order of GSPS. ROM encoder [19]-[20] and fat tree encoders [21] are usually employed as code converters but these converters convert thermometer code into the 1-out-of-n code and at last it converts into binary code.

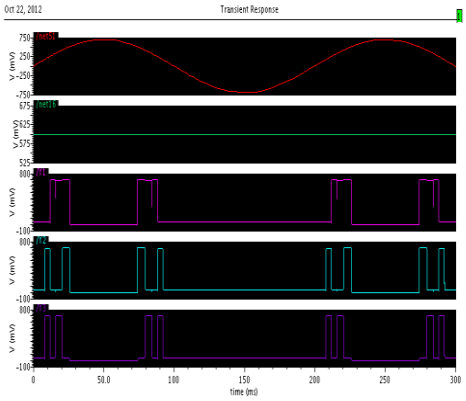

Fig 2.Transient behaviour of flash ADC

Figure 2 shows the Flash ADC transient output analysis of "3" bit flash ADC for analog input signal VSIN of 5000 Hz frequency. Bit "0" represent the LSB and bit "2" represent the MSB of the binary digital output of "3" bit flash ADC.

B. Fat-Tree Encoder

By help of these equations we have design Fat-tree encoder.

$$d_0 = (a_{1+}a_3) + (a_{5+}a_7)$$

$$d_1 = (a_{2+}a_3) + (a_{6+}a_7)$$

$$d_2 = (a_{4+}a_5) + (a_{6+}a_7)$$

A fat-tree encoder has been designed to convert the encoded signal into n bit data this data is digital which is in binary code [22]-[23]. The output of converters is given in the encoded form but it is functioning of fat tree encoder that it converts the giving encoded signal into digital data. With this function the TC-to-BC encoding is carried out into two stages in the fat tree encoder. Fat tree encoder converts the data in many stages: the firsts on stage convert into the thermometer code to one-out-of-N code then encodes is the same address's decoder output. This code converts N bit parallel. The second stage converts the one-out-of-N code to binary code using the multiple trees or fat tree circuit signal delay is O(log2 N)after it ROM circuit signal delay is O(N)[24].

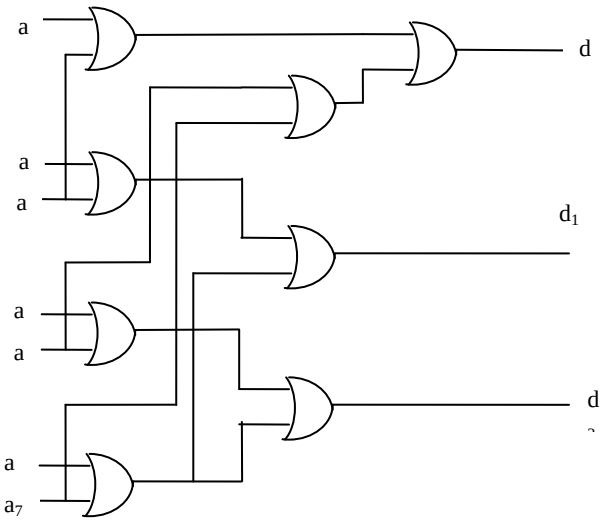

Fig 3.Schematic of Fat-tree encoder

In this way the Signal encoding delay is O (log1:5 N). A fat tree encoder performs better as has signal delay of "0" this is the speed is improved by a factor of 2 when we use a fat tree encoder. The fat tree encoder is a very good solution for the little problem in high speed ADCs.

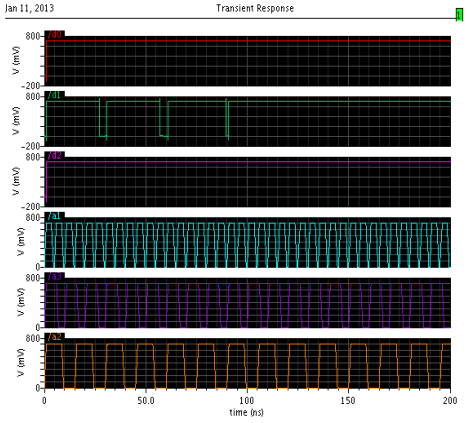

Fig 4.Transient Responce of Fat-tree encoder

C. Comparator

Comparator is a component of analog-to-digital converter, plays important role to achieve overall good performance. The appropriate way to minimize the power consumption is reduce the supply voltage at minimal level high speed and high resolution is performance criteria that decide comparator is important element for data converter. It is used in front-end signal processing and electronics components [25] Lowering the input impedance is effective to improve better performance of comparator [26]-[30].Inverter based comparator is reduce offset error [31]. The Flash ADC performance of depends on comparator input signal without jitter [21]. The number of transistors is reduced from the

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adder circuit with the help of pass transistor logic, but the circuit is suffering from static power dissipation [29].

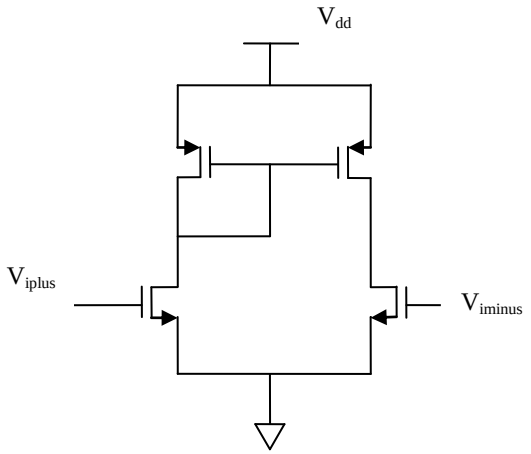

Fig 5. Schematic of comparator

III. DIODE BASED STACKING POWER GATING TECHNIQUE

Diode based stacking power gating scheme is improved gating technique to reduce the leakage current and ground bounce noise efficiently. The Stacking sleep transistor (ST1 & ST2) is used in this technique as shown in fig. 6. The diode based stacking power gating technique relies on different component that is described below:

- Transistor ST1 and ST2 are the sleep transistor.
- T3 is the control transistor.
- TG is the transmission gate.
- ΔT is a time delay between T1 and T2.
- C1 is the capacitor.

Whenever the circuit is operated in standby mode, leakage current become considerably effective and when the circuit is done transition from sleep to active and vice-versa. Ground bounce noise become concerned factor that must be reduce for better operating condition of device. Diode based stacking power technique employ three mechanism to reduce the current flow from sleep transistor. Diode based stacking power gating technique has three operating mode which is shown below.

A. Active Mode

Sleep transistor's ST1 & ST2 always remain in ON condition during the active mode operation and transistor S1 that behave as control transistor is OFF. ST1 & ST2 both transistors offer very low resistance level (R1ON & R2ON). C1 is intrinsic capacitance that become (virtual ground node) & C2 is external capacitance become (intermediate node) between ST1 & ST2 transistors.

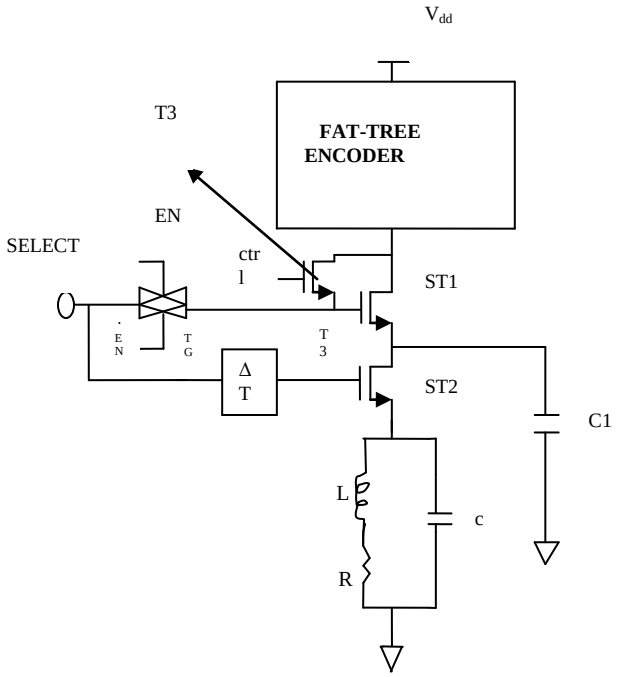

Fig 6. Fat-tree Encoder design with diode based stacking power gating technique.

$$Voltage\ across\ C1 = V_{c1}(active\ mode) = V(V_{R1ON} + V_{R2ON}) \quad (1)$$

$$Voltage\ across\ C2 = V_{C2}(active\ mode) = V(R2_{ON}) = 0 \quad (2)$$

B. Standby Mode

Sleep transistor's ST1 & ST2 are OFF in standby mode therefore

$$\text{Voltage across C1 (standby mode)} = V_1 \quad (3)$$

$$\text{Voltage across C1 (standby mode)} = V_2 \quad (4)$$

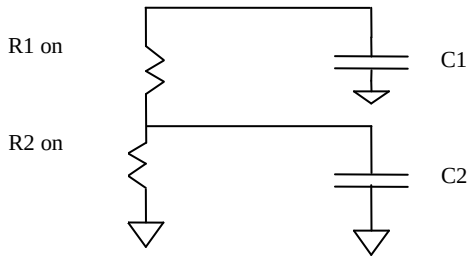

Fig 7 Equivalent circuit of sleep transistor ST1 and ST2 in active mode

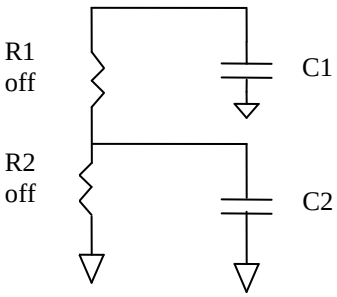

Fig 8 Equivalent circuit of sleep transistors ST1 and ST2 in standby mode.

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Positive potential is generated at the intermediate nodes having different effects which are described below:

- Gate to source voltage (Vgs1) is applied at ST1 transistor became negative.
- Negative potential at body to source terminal (Vbs1) of control transistor T3 cause body effect.
- Negative potential at body to source terminal (Vds1) of sleep transistor ST1 decline, affecting in lower drain induced barrier lowering (DIBL).
- Drain to source potential (Vds2) of sleep transistor ST2 is lower as compared to control transistor T3, occur due to voltage drop across ST1. This mainly reduces the drain induced barrier lowering (DIBL).

C. Sleep to Active Mode

When the circuit is operated in sleep-to-active mode & vice-versa then ground bounce noise reduction is reported in the circuit. During first stage sleep transistor (ST1) behave as diode by turning on the control transistor (T3) that become forward biased stage which is connected across drain and gate of transistor (ST1). By turning the control transistor, reduction in the voltage fluctuation on the ground and wakeup time occur, therefore initially transistor (ST1) turn ON and control transistor T3 must also ON but after some delay to reduce the ground bounce noise. During the second stage, sleep transistor works as normal manner when the control transistor (T3) is OFF. In sleep to active mode, control transistor T3 is ON and sleep transistor ST2 is turned ON after some delay to reduce the ground bounce noise Ground bounce noise is reduced effectively during this mode of operation.

IV. SIMULATION AND PERFORMANCE CHARACTERSTICS

A. Active power simulation

Whenever the circuit is operated in supply mode and power is dissipated during the operation and supply mode by the circuit is known as active power. Dynamic power and Static power of the circuit comprises the active power. We had calculated the active power of the circuit at different voltages for the 45nm technology. Active power also calculated by equation [32].

$$P_{act} = P_{dyna} + P_{stat} \quad (5)$$

$$= P_{swi} + P_{s-c} + P_{leak} \quad (6)$$

$$= (\alpha_{0\to1} \times C_{load} \times V_{dd}^2 \times f_{clock}) + (I_{s-c} \times V_{dd}) + (I_{leak} + V_{dd}) \quad (7)$$

Where, Pact=active power, Pdyna=dynamic power, Pstat= static power, Pswi= switching power, Ps-c=short circuit power, Pleak=leakage power, Cl = capacitance at load, fclock = frequency at clock, α = switching activity, Is-c = current when circuit is short, Ileak = leakage current, Vdd = supply voltage

Table I: Active Power of Fat-Tree Encoder

Different voltages(volts)	Active power(uw)
0.5	45.22
0.7	46.11
0.9	46.72
1.1	50.05

It clearly indicate that fat-tree encoder with diode based stacking power gating scheme , active power is greatly reduced as compared to simple encoder design. Reduction of 16 % active power achieve after using diode based stacking power gating technique.

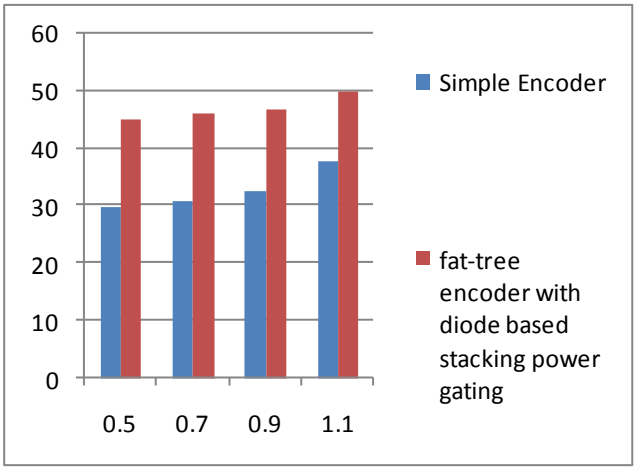

Fig 9. Active Power Dissipation of Fat-tree encoder

B. Leakage current simulation

Leakage current of the Encoder is estimated during the standby mode. To estimate the leakage current of the Encoder, NMOS transistor is required to measure the leakage current that is connected at the pull down network below the whole circuit. Sleep transistor is OFF for this technique whenever leakage current calculation is analyzed. Leakage current is derived and calculated by the equation given below [33].

$$I_{leak} = I_{sub-thr} + I_{gat-ox} \quad (8)$$

Where, Isub-threshold = sub-threshold leakage current, Igat-ox = gate-oxide leakage current.

$$I_{sub-threshold} = K_A W e^{\frac{-V_{th}}{nV_\Theta}} (1 - e^{\frac{-V}{V_\Theta}}) \quad (9)$$

Where, KA and n are experimentally derived, W = gate width, Vth = threshold voltage, n = slope shape factor, VΘ = thermal voltage.

$$I_{gat-ox} = K_B W (\frac{V}{T_{ox}})^2 e^{\frac{-\alpha T_{ox}}{V}} \quad (10)$$

Where, KB and α are experimentally derived, Tox = oxide thickness

Table 2. Describe the leakage current analysis at different voltages

Different voltages(volts)	Leakage current(nA)
0.5	113.40
0.7	164.37
0.9	202.48
1.1	287.93

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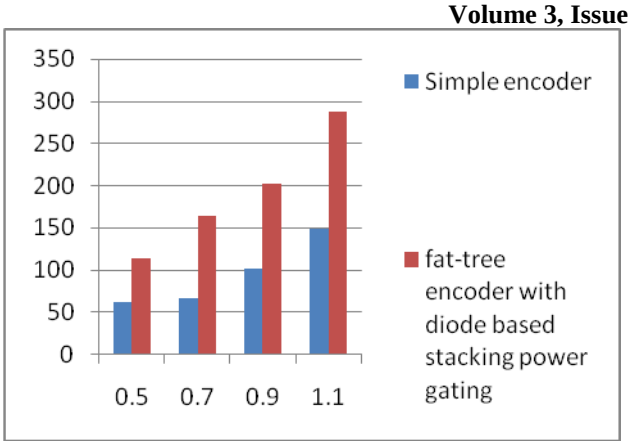

Fig 10.Leakage current of 3 bit flash ADC

It clearly indicates that fat-tree encoder with diode based stacking power gating scheme, active power is greatly reduced as compared to conventional design. Reduction of 82 % leakage current achieve after using diode based stacking power gating technique.

C. Leakage power simulation

During standby mode the leakage power of the circuit is measured. It explains that how much percentage of power is wasted by the whole circuit during off state condition when there is no supply. Leakage power is the product of the leakage current and supply voltage. The basic equation of leakage power is realized by Eq. (12) [34]

$$P_{leak} = I_{leak} \times V_{dd} \quad (11)$$

Where, Ileak = leakage current, Vdd = supply voltage.

Table 3. Describe the leakage current analysis at different voltages

DIFFERENT VOLTAGES(VOLTS)	LEAKAGE POWER(NW)
0.5	56.7
0.7	115.05
0.9	182.23
1.1	316.723

It clearly indicates leakage power is reduced to 73% with diode based stacking power gating scheme.

D. Ground bounce noise reduction

Ground bounce noise produced by the diode based stacking power gating scheme is characterized in this section. We used a well-characterized 40-pin Dual In-Line Package (DIP - 40) model in this paper to evaluate the ground bounce noise [35]. The model of DIP-40 is shown in figure. Ground bounce noise occurs when the circuit is going from sleep to active mode and vice-versa. The noise immunity of a circuit decreases as its supply voltage is reduced.

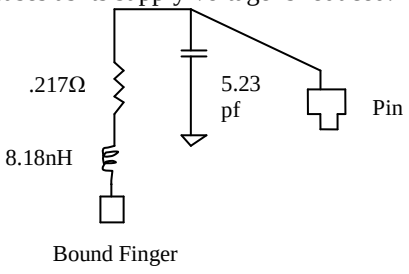

Fig 11. DIP-40 package pin ground bounce noise model

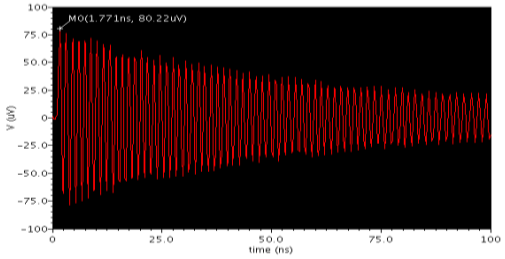

Fig 12. Showing ground bounce nosie of fat-tree encoder with diode based stacking technique

Ground bounce noise is reduced effectively in designed fat-tree encoder with diode based power gating technique as compared to conventional design. Ground bounce noise is reduced up to 73 % with this technique.

V. CONCLUSION

In this paper low leakage "3" bit flash ADC is designed for signal processing and communication systems and design of Fat-tree Encoder with improved diode based stacking power gating technique describe for ground bounce noise analysis. A high performance diode based stacking power gating technique has been used to minimize the ground bounce noise and control the leakage power during the sleep to active mode transition. The ground bounce noise is restricted with the help of a delayed select signal associated by using a stacked sleep transistor. In diode based stacking power gating technique, the ground bounce noise is controlled by using a stacked sleep transistor with the help of a delayed select signal. The leakage power and leakage current are reduced by 79% and 82% with diode based stacking power gating technique in comparison to Simple Encoder. Ground bounce noise is reduced by 75% with diode based stacking power gating technique in comparison to Simple Encoder. Active power is reduced up-to 14% with diode based stacking power gating technique.

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