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Obstacle Avoiding Delay Equalization for Rectilinear Clock Tree Routing based on a Game Theoretic Approach

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Abstract*— Clock skew minimization plays an important role in VLSI interconnect design to assure enhanced performance of a chip. In this paper, we propose an Obstacle avoiding Rectilinear Clock tree construction algorithm. IP blocks, transistor cells, elongated wires, and redundant vias present on-chip are treated as obstacles, and cause extra delay around their boundaries while performing routing. Our proposed algorithm focuses on delay equalization at all the sink terminals from the source, avoiding obstacle edges. Delay equalization problem is formulated in a non cooperative game theoretic framework, where all the sink terminals are treated as players. The proposed method is maneuvered as follows. (1) Initially, the entire layout is divided into smaller rectangular or square subzones, called tiles, containing subset of sink terminals. (2) Next, center of masses (CMs) of the tiles are treated as individual players to play several strategies. Delay equalization is done in each CM sequentially by playing the set of predefined strategies. Delay difference or clock skew is treated as the payoff matrix, which it optimized/minimized in several iteration of the play. Nash equilibrium is also achieved by optimizing the payoff matrix. (3) Finally, the game is played in each tile to find out Nash equilibrium, where the sinks belonging to each tile are treated as the players during local game playing. This two stage process of global delay equalization at CMs, followed by local optimization leads to clock skew minimization in all the sink terminals from the source terminal. We adopt Elmore delay formula to calculate delay of a routing path, considering the resistive (R) and capacitive (C) effects of a wire. Proposed algorithm is run on some recent benchmark suits, and experimental results are quite encouraging.

Index Terms—**Clock Tree, Obstacle, Obstacle Avoiding Rectilinear Clock Tree Construction, Clock Skew Minimization, Elmore Delay, Game Theory.**

I. INTRODUCTION

The fundamental goal of the routing step is to connect every net successfully and to resolve resource contentions. In modern VLSI design, this could be an exceedingly complex problem if the process was done in a single step. There could be millions of elements and nets integrated on a single chip increasing the design complexity [1]. Construction of Rectilinear Steiner Tree (RST) takes a vital role in VLSI physical design. It is substantially important for global as well as detailed routing phases of physical design for congestion estimation and wire length computation. Also, routability of a design can be verified by construction of RSTs for every net independently, so as to avoid all blockages such as pre-routed nets, buffer, I/O ports and many more. Constructing rectilinear Steiner minimal tree (RSMT) in presence of large macro, IP blocks and pre-routed nets, treated as obstacles, is a progressive research area these days. The problem is defined as obstacle-avoiding Rectilinear Steiner tree (OARST) routing problem. It was proved that RSMT problem is an NP-complete problem [16], hence constructing RSMT in presence of obstacles is also an NP-complete problem. The objective of the routing problem is dependent on the nature of the chip. For general purpose chips, it is sufficient to minimize the total wire length, while completing all the connections. For high performance chips, it is important to route each net such that the net meets its timing budget. Usually routing involves special treatment of nets such as clock nets, power and ground nets. In fact, these nets are routed separately by special routers [4]. Now-a-days, focus is made so that signal originating from the same source reaches every pin of a time critical net in almost equal time. That is, the delay of signal reaching every pin of a net through a series of gates having internal resistances and wire capacitances, and source capacitance has to be minimized. This condition is stringent for critical nets [14]. Difference in time to reach the clock pulse at the different sink terminals is known as clock skew. Our goal in this work is to minimize the clock skew. This can be done at local level i,e, compute clock skew only for a pair of "local clock sinks", referred to as Local Clock Skew (LCS), where local clock sinks are all the sinks present within a distance less than "local skew distance" typically 600um as an example [9, 10]. The clock skew minimization can also be done for all the pins (critical sinks) within the entire grid, thereby forming a clock tree. This is termed as global delay equalization. Popular clock tree construction algorithms are H-tree or MMS algorithms that construct global clock trees with uniform node distributions [4]. Global clock routing in presence of obstacles is a new domain of research in recent days. Rectilinear Shortest path routing in presence of rectilinear obstacles was performed in [17]. FORST [23] was a well-known three-step heuristic algorithm that constructed rectilinear Steiner tree in three stages by partitioning, grouping and connecting groups by applying a meta heuristic search technique. Some contemporary works on obstacle-avoiding rectilinear Steiner tree routing were cited in [8], [6], [22], and [25]. However, none of the work focused on solving clock tree construction problem in

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presence of obstacles. In this paper, we propose a game theoretic approach to solve the rectilinear clock tree construction problem in presence of obstacles. Our proposed algorithm is summarized as follows.

- Partition the whole layout area into smaller rectilinear regions called tiles, update the obstacle edge information in each tile.
- Count terminals in each partitioned area (tile), and find center of mass (CM) of every tile using arithmetic mean of the terminal.
- Required Arrival Time (RAT) is determined, based on the distribution of CMs, and is culminated for delay equalization in CMS.
- Each CM then plays a non-cooperative game sequentially adopting their strategies, and optimizing payoff function in each iteration. Delay equalization is done to each CM, choosing required rectilinear path.
- Local delay among all the sinks in each sub zone is equalized next to achieve zero skew in all the sink nodes or pins. In this stage, sinks in each tile acts as a non-cooperative game player to optimize the payoff function.

The rest of the paper is organized as follows. Section II provides a brief survey on clock tree routing. Section III poses a preliminary idea of delay tree construction, followed by problem formulation in Section IV. Game theoretic approach adopted in our present work is deliberated in section V. Section VI describes the proposed method with formal description of the algorithms. Time and space complexity analysis for Nash equilibrium is done in Section VII. Experimental results are cited in Section VIII. Finally, Section IX concludes the paper with possible future directives.

II. LITERATURE SURVEY

In [13], the authors develops a branch and bound method to minimize the Elmore sink delay. Their result restricts the Steiner node in an optimal Elmore delay rectilinear Steiner tree construction. They generalize a theorem of Hanan for finding the minimum cost of Steiner tree. They use the critical sink problem formulation, since it is found that a significant timing improvement is achieved by minimizing delay to single critical sink. In optimal Steiner tree routing they emphasize on reducing wire-length, but they simultaneously reduce the skew. In this technique, the authors followed divide and conquer method, where they first divided the whole tree in some sub trees and minimized skew from them and then merge all the sub trees to form an optimized tree. If any kind of problem further existed, they minimized it using BBSORT-C algorithm. in [22], the authors proposed nice algorithm for Rectilinear Steiner tree construction in presence of obstacles. However, they did not consider critical sink delay. in the OARSMT problem [8], the authors define a set V of n terminals on the 2-D plane and a set B of m rectangular obstacles. No obstacle can overlap with each other, but they can be line touched at the boundary. The objective of the problem is to give an obstacle-avoiding tree with the shortest length that connects all of those n terminals using only horizontal and vertical lines. This tree is known as an Obstacle Avoiding Rectilinear Steiner Minimal Tree (OARSMT). in [11], the authors propose a novel clock-tuning algorithm, ClockTune, which considers buffer insertion/sizing and wire sizing at the same time, while maintaining the clock tree zero skew Clock distribution is crucial for timing and design convergence in high-performance very large scale integration designs. In this paper, the authors present ClockTune, a simultaneous buffer insertion/sizing and wire-sizing algorithm which guarantees zero skew and minimizes delay and power in polynomial time. The algorithm ClockTune achieves 45 times delay improvement for buffering and sizing an industrial clock tree with 3101 sink nodes on a 1.2-GHz Pentium IV PC in 16 minutes, compared with the initial routing. This algorithm can also be used to achieve useful clock skew to facilitate timing convergence and to incrementally adjust the clock tree for design convergence and explore delay-power tradeoffs during design cycles. Moreover, if the clock-routing encounters design changes, ClockTune is able to re-balance the clock tree by local adjustment. in [18], the *associative skew clock routing problem* was solved by reusing existing techniques including the difficult instances, based on a more accurate and popular delay model. Experimental results as shown by the authors prove that their algorithm can reduce the total clock routing wirelength by 12% on average compared to greedy-Deferred-Merge Embedding (DME) algorithm that is one of the best zero skew routing algorithm. Clock network was used to emphasize on both performance and power efficiency of integrated circuits. A common goal of clock network synthesis is to minimize clock network size subject to skew constraints. The authors introduced the associative skew clock routing problem which seeks a clock routing tree such that zero skew is preserved only within identified groups of sinks. The associative skew problem is easier to address within current EDA frameworks than useful-skew approaches, and defines interesting tradeoffs between the traditional zero-skew clock routing problem and the Steiner minimum tree problem. The authors cited an efficient and optimal method of merging two zero-skew trees such that zero skew is preserved within the sink sets of each tree. The exact zero-skew clock routing algorithm [21] was based on Elmore delay model. The results have been verified with accurate waveform simulation. The author first reviewed a linear time delay computation method. Experimental results show an 8% to 15% wire length reduction over some previous constructions. A recursive bottom-up algorithm was then proposed for interconnecting two zero-skewed sub trees to form a new tree with zero skew. The algorithm can be applied to single-staged clock trees, multi-staged clock trees, and multi-chip system clock trees. The approach is ideal for hierarchical methods of constructing large systems. All

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subsystems can be constructed in parallel and independently, then interconnected with exact zero skew. The algorithm constructs a bounded-skew tree (BST) in two steps. Firstly, a bottom-up phase to construct a binary tree of shortest-distance feasible regions which represent the loci of possible placements of clock entry points. Secondly, a top-down phase to determine the exact locations of clock entry points. in [15], two approaches, named sequential routing and concurrent routing were proposed to serve multiple nets. In the first approach the nets were ordered according to the number of pins contained in it, bounding box radius or criticality of the nets. Then the nets were routed independently. An example illustrating exploitation of such ordering of nets appeared in several papers such as by D. T. Lee and C. F. Shen. The paper proposed a method for avoiding intersection between nets. The proposed method was a balanced tree based algorithm that generated magic numbers for net ordering. Global routing for modern large-scale circuit designs has attracted much attention in the recent literature. Most of the state-of-the-art academic global routers just work on a simplified routing congestion model that ignores the essential via capacity for routing through multiple metal layers. Such a simplified model would easily cause fatal routability problems in subsequent detailed routing. To remedy this deficiency, a more effective congestion metric that considers both the in-tile nets and the residual via capacity for global routing is presented in [5]. Experimental results show that their global router can achieve very high-quality routing solutions with more reasonable via usage. In this paper, the authors have derived congestion metric, and dynamic via capacity for global routing. The metric practically considers via capacity as well as the in-tile nets. With this metric, the authors have developed a new global router that features two novel effective routing algorithms, aerial-monotonic routing and multisource multi-sink escaping point routing, for congestion optimization. In particular, the linear-time escaping point routing algorithm is optimal in the sense that it achieves the theoretical lower-bound complexity. Experimental results have shown that their global router can achieve better routing solutions with more reasonable via distribution that can benefit and correctly guide subsequent detailed routing. For the experiments considering dynamic via capacity on the ISPD'07 and ISPD'08 benchmarks, their router achieved the best overall results for the total overflow (including the via and wire overflow) and the total via overflow. It should be noted that the total via overflow for the bigblue2 circuit is zero since the wire-capacity constraints on this circuit are very critical; the bigblue2 circuit contains 23978 zero-capacity routing edges while bigblue4 contains only 35 zero-capacity edges and the others contain no zero-capacity routing edges. The experimental results show the high quality and superiority of their router. Here, authors' prioritized order is as follows: 1) the total overflow; (2) the maximum overflow; and 3) the total wire length. In [7], the authors integrated clock network synthesis within global placement by optimizing register locations. They proposed the following techniques: (1) obstacle-aware virtual clock-tree synthesis; (2) arboreal clock-net contraction force with virtual-node insertion, which can handle multiple clock domains and gated clocks; (3) an obstacle-avoidance force. Their work was validated on large-size benchmarks with numerous macro blocks. Experimental results showed that their software implementation, called Lopper, prunes clock-tree branches to reduce their length by 30.0%- 36.6% and average total dynamic power consumption by 6.8%-11.6% versus conventional approaches. Literature survey shows that very less work was done on clock tree implementation, considering the effect of obstacles. Also using *game theory* is a new domain of work in this realm. This is the source of our motivation towards the present work.

III. PRELIMINARIES

Accurate delay estimates are critical for performance prediction, the simplest estimate being the Manhattan distance between circuit nodes. However this simplest estimate fails to give accurate delay values in electrical circuits, as the electrical components of a conducting wire dominates over that of electrical gates in the deep submicron range (DSM) of design. Also considering lumped RC structure as an interconnect delay model provides a crude approximation [4], which fails to attain the exact performance measure. Hence researchers go for parameterized distributed delay models incorporating different electrical parameters like resistance (R), inductance (L), capacitance (C), and conductance (G), in constructing interconnect model at high frequency range of operation. In our work, we used distributed RC model to estimate critical sink delay based on Elmore Delay model [2], without considering the high frequency effect. The Elmore delay, $\partial_{ED}(n_i)$ between source n_0 and sink n_i is then,

$$\partial_{ED}(n_i) = r_d \times C_0 + \sum_{e_j \in path(n0, ni)} r_{ej} \times (c_{ej}/2 + C_j) \quad ---(1)$$

Where, r_d, C_0 are the resistance and capacitance of the source n_0, r_{ej} and c_{ej} are resistance and capacitance of the edge e_j respectively, and are proportional to the length of the edge e_j. Each edge in the global tree structure is designated using π circuit model, combining resistance (r) and capacitance (c). Resistance r is placed in series with two capacitances c/2 in parallel to complete the electrical model of an edge. Our proposed work of clock tree construction is based on this π model to construct global as well as local clock tree. High performance clock tree routing is another challenge in today's DSM range of manufacturing [10]. Most of the clock tree routing focuses on reaching a predefined clock skew at all the sink terminals, or making a zero skew tree structure [20]. The popular delay structure followed is Elmore delay, as it inculcates less computational complexity, than other exact delay models like HSpice [24]. In the next section, clock tree routing problem is elaborated with proper definitions.

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IV. PROBLEM FORMULATION

In synchronous VLSI circuits, component speed is limited extensively by clock skew. In any electronic circuit, clock skew, T_{Skew} is defined to be the difference in the arrival time between two sequentially-adjacent registers or components or pins of the circuit. Given two sequentially-adjacent registers R_i and R_j with clock signal arrival times at register clock pins as ∂T_i and ∂T_j respectively, clock skew can be defined as:

$$T_{Skew}(i,j) = \partial T_i - \partial T_j \quad \text{---------- (2)}$$

∂T is calculated using Equation (1).

So, a clock tree needs to be formed so as to connect all the equipotential pins of the circuit maintaining minimum or optimum clock skew at least within local skew distance (LCS). Clock skew minimization can be done in various ways, like wire sizing, buffer insertion, gate sizing, as is discussed in Section II. In this work, we adopt a rectilinear path construction technique with efficient Steiner point insertion, to minimize clock skew.

Obstacle Avoiding Clock tree Construction:

Given a set of rectangular obstacles (M), and a number of sink nodes (N), our aim is to connect all the sink nodes using rectilinear routing path, such that there is no intersection between the obstacle edges, and routing paths. Clock tree routing is aimed to route all the sink terminals from a predefined source location. Our goal is to reach all the sinks nodes from the source terminal at the same time, i.e. minimization of clock skew, avoiding the edges of the obstacles. Two types of clock trees are constructed to analyze the performance of our algorithm. Local clock tree is the tree constructed using the sink terminals placed at a distance 600 µm from the obstacle edges, and considers local clock skew (LCS) to be minimized. Next, global clock tree is constructed reaching all the sink terminals on the layout beyond LCS distance, and skew minimization is done on the global scenario. Local clock skew minimization is done based on a specified LCS distance, supplied in the benchmarks, and global clock skew minimization is done based on a "Required arrival time" (RAT) value. RAT is calculated based on the distribution of the sink nodes on a layout using Equation (1), and the global clock tree structure formed subsequently tries to reach that RAT value in an iterative manner.

Goal: Reaching all the sinks nodes from the source terminal at the same time, i.e. minimization of clock skew, avoiding obstacles.

V. GAME THEORETIC APPROACH

We discuss now few important definitions and concepts of game theory related to our work.

Game theory is the mathematical modeling of different strategy profiles of rational decision makers.

Cooperative game is a type of game where the players, in spite of competing, cooperate with each other in order to achieve a common goal. Players of a cooperative game are not only mere competitors. Rather, they form 'coalition' to help each other to earn better payoffs.

Non cooperating game is a type of game where all the players of the game intend to choose the best strategy for them in order to maximize the individual payoffs by conflicting each other.

In a game, *payoff matrix* is a snapshot of different player names, their strategies and the payoffs earned by the players against all possible strategies. Actually, payoff is the measure of the benefit obtained by a player for a particular strategy or a set of strategies taken by that player. Our proposed clock tree construction method is manifestation of non-cooperative finite game playing. Non-cooperative game can be of two types, (1) normal game and (2) sequential game [20]. Sequential game playing is adopted in our approach to construct Clock tree. Non-cooperative tree construction is guided by choosing Steiner points for a sink independent of the other sinks choice. The aim is to reach all the sinks at nominal skew or zero skew value by choosing a strategy that may not be influenced by the choice of other sink node. Strategy S is defined as the possible combinations of path movements to play the game, $S = \{S_1, S_2, ...S^*, ..., S_n\}$. For non-cooperative game theory, choices need to be made among these strategies to reduce clock skew in each iteration. Hence, payoff function in our work is chosen as the minimal or zero clock skew. Players are chosen succinctly based on the proposed structure of the game, which plays the strategies and tries to optimize the payoff function. Clock skew can be minimized, or reached to zero by proper choice of routing paths. There exists a solution, which delivers optimal clock skew, after playing several strategies, and the state of the optimal solution is called Nash equilibrium, achieved by playing the strategy S*. At this point of the game, no improvement in payoff function can be made by changing the strategy of individual player. It is proven in theory that obtaining Nash equilibrium lies between P and NP, depending on the problem formulation [3]. We have modeled the Obstacle avoiding clock tree construction problem as a finite game, with restricted choice of strategies to reduce the space and time complexity of our algorithm.

VI. PROPOSED METHOD

Our proposed method starts executing with the information of rectangular obstacle zone, and pin locations on a layout area. Routing area is the entire layout area, apart from the rectangular obstacle zones. Fig. 1 demonstrates how the entire routing area is partitioned into tiles, each one of nearly equal square area. Here the black points indicate the sink, red dots indicate Center of Mass (CM) for every tile, and yellow dot indicates source and red rectangles denote blockages for routing. Initially, rectangular tiles are created by drawing horizontal and vertical lines, dividing the entire layout area into equal zones. A data structure is maintained to recognize the existence of obstacle zone in each tile. During running a horizontal or a vertical edge, care is taken if the line is passing through any edge, or across any obstacle zone. If that happens, the array obs_edge[] in algorithm 1 is updated with

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the coordinate of the edge of the obstacle. Number of pins associated with each tile is accounted during drawing the horizontal and vertical lines also. Tile creation procedure is explained in Algorithm1. Then, for every tile, Center of Mass (CM) of all the nodes is computed as the arithmetic mean of all the node coordinates available within a tile. This procedure is revealed in Algorithm 2. Our proposed Clock tree construction method is guided by Rectilinear Steiner Minimal tree (RSMT) construction algorithm [19], where routing paths can go either in horizontal or vertical direction. Sequential game playing is

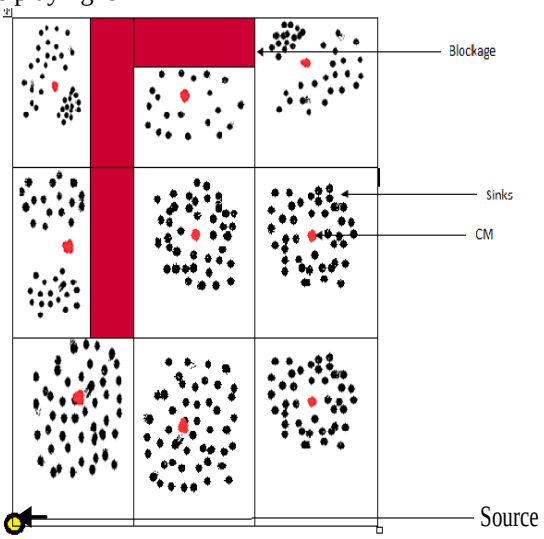

Fig. 1 Rectangular Tile Creation

Adopted in this step to connect all the CMs of the tiles to the source. This stage of game is treated as global game playing, to connect all the CMs from the source node, with almost equal delay. All the CMs are sorted in descending order of rectilinear distance according to their coordinates from the source location. As the rectilinear routing architecture is chosen, the strategies of the players are restricted to four moves, S = {SN, SS, SR, SL}, these are the movement of the routing paths in the vertical upward and downward directions (SN, SS), and horizontal forward and backward directions (SR, SL). The CMs of all the tiles are the possible players in the game, who play in non-cooperative manner without the knowledge of the other player's payoff. The CM, which is furthest apart from the source location, is connected first by proper choice of strategies from S, and hence finding optimal delay to reach the CM. The delay involved in traversing this distance is termed as Required Arrival Time or RAT. The path constructed so far is treated as the main trunk of the routing tree structure. During choosing possible strategies for routing direction, care is taken that the routing path does not intersect with any obstacle edge recorded previously. The delay of signal to reach the furthest CM is calculated by the formula in Equation (1). This path encounters maximum delay. Hence signal from the source should reach the other CMs at a time equal to the RAT for main trunk to equalize delay in all the CMs. Next, all the CMs are connected to the source in a sequential manner, choosing each CM from the sorted array. This is done by optimally choosing the Steiner points and rectilinear routing path at every point using Game theory.

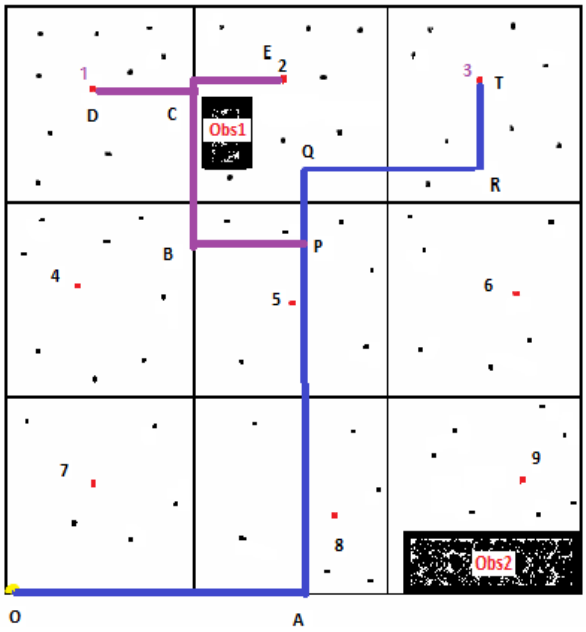

Fig. 2 Routing Center of Mass (CM) in each Tile

The opportunities available at every point is exploited and balanced against all the strategies optimally. Every CM connects to the source in a greedy manner neglecting the presence of all other CMs, by choosing the strategy that provides with optimal payoff in an iterative basis. Optimal payoff signifies reaching the signal to each CM within RAT. After a few iterations Nash Equilibrium is achieved and an optimal solution is found, where every CM is connected to the source by a path having a delay nearly equal to RAT. Under Nash equilibrium, the game G may be represented as, $G = \{S_1, S_2, \ldots S_N; P_1, P_2, \ldots P_N\}$, a non-cooperative game with N players having P as the payoff matrix. The set S_i contains all the strategies, and P_i contains all the payoff values for the player i. The payoff values are calculated from the difference between RAT and delay at the i^{th} CM, in every iteration. Once Nash equilibrium is reached playing strategy $s^* = (s_1^*, s_2^*, \ldots s_3^*)$, Payoff matrix reaches its minimal value, with,

$$P_i(s_1^*, s_2^*, \ldots, s_i^*, \ldots, s_N^*) < P_i(s_1^*, s_2^*, \ldots, s_{i-1}^*, s_i^*, s_{i+1}^*, \ldots, s_N^*) \quad \text{----------(3)}$$

Equation (3) holds $\forall s_i \in S_i$. Hence, P cannot get better playing other strategies, once Nash equilibrium is reached.

In Fig. 2, the path OAPQRT corresponds to RAT connecting the farthest CM labeled 3. All other CM s labeled 1 through 9 must be connected by paths having delays almost equal to RAT. Such as the paths OAPBCD and OAPBCE, connecting CM 1 and 2 respectively, are almost equal to RAT. In this manner, we can connect all other CM by balancing the delay through the path from source.

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Algorithm1. Tile creation algorithm

Input: Layout Area; Obstacle left corner coordinates, width and height; Pin locations;
Output: Rectangular tiles with specified boundary coordinates

1. Obs_edge[]:=0; Tile_bound:= 0

(*Initialization)

2. Divide the entire routing space into equal sized tiles of size $t = dx/ N_{tx}$ by drawing horizontal and vertical lines

where $dx = x_n - x_0$, N_{tx} = Number of tiles chosen in x direction, x_n, x_0 are the maximum and minimum x coordinate of the grid.

3. For each tile in grid

4. Mark the boundaries of the tiles using $x_{i+1} = x_i + t$, $y_{i+1} = y_i + t$
5. Update Tile_bound[];
6. Update obs_edge[];
7. End For

Algorithm2. Centre of Mass calculation for each tile

1. For each tile in grid
2. Calculate the mean of the points as

$X_{mean} = \Sigma x /n$, $Y_{mean} = \Sigma y /n$,

where n= Number of nodes within the tile.

3. Name the coordinate (X_{mean}, Y_{mean}) as Centre of Mass (CM) for the tile.
4. End For

After connecting all the CM s to the source in almost equal Delay, all other sink nodes may be connected to the corresponding CM of their tiles by balanced Rectilinear Steiner tree or H tree construction. In this stage game theory is played locally, with all the nodes in a tile treating as individual player. Each player plays its own strategy to find suitable bend, adding Steiner point in routing path to connect to the corresponding CM to find optimal Payoff function. Thus, all the nodes within the routing area are delay balanced with respect to the source. Hence, clock skew may be minimized to the extent of zero. Algorithm3 and Algorithm4 present a formal description of Obstacle avoiding clock tree construction algorithms. The worst case time complexity to achieve Nash equilibrium for M players with S strategies is $O(M * S^M)$ [12]. In our proposed game theoretic approach, total time complexity is calculated in the following three steps.

Algorithm3. Routing all the CM with respect to the source

1. Set lower left coordinate of the layout as the source
2. Sort the CMs and assign criticality to them
3. Play strategy S:= {SN, SS, SR, SL} to route the farthest CM (CM_n)
4. Construct RSMT with optimal payoff and calculate delay using Equation (1)
5. Set RAT:= Delay of RSMT of main trunk
6. For each CM_i
7. Choose strategy to connect Source → CM_i
8. Play S:= {SN, SS, SR, SL} such that $\sum (\partial_{xi} + \partial_{yi})$ approach RAT using suitable bends guided by Strategy choice and adding suitable Steiner node where,

∂_{xi} = displacement in x from source to CM_i
∂_{yi} = displacement in y from source to CM_i
(Summation accounts for total delay of the path constructed so far)

9. End For

Algorithm4. Routing all the points with respect to the CM

1. For each CM_i (for each tile)
2. Find the farthest point P_j with $\max(dx_j + dy_j)$
   where $dx_j=(CM_{ix} – p_{jx})$ and $dy_j=(CM_{iy} – p_{jy})$
3. Route the farthest point P_j from CM_i using RMST
4. Manhattan distance of P_j converted to delay value using Equation (1) is considered to be RAT_1
5. For each points P_k
   Connect $CM_i \rightarrow P_k$ such that
   $\sum (\partial_{xk} + \partial_{yk})$ approaches RAT_1 using suitable bends guided by heuristics and adding suitable Steiner nodes
   where ∂_{xk} = displacement in x from CM_i to P_{kx}
   ∂_{yk} = displacement in y from CM_i to P_{ky}
6. End For
7. End For

VII. TIME AND SPACE COMPLEXITY

Input to the proposed algorithm described in Section VI, is number of obstacles M and number of pins or sink nodes N. In the first part of the algorithm, tile creation using horizontal and vertical lines checks the edges or corner coordinates of the obstacles to update the array obs_edge[], which takes into account the presence of obstacle regions in every tile. This

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execution requires O(M × 2 × T) ≈ O(M × T) times, where T is the number of tiles created. The term 2 comes due to checking of the obstacle edges for both the horizontal and vertical lines associated with a tile. If it is assumed that the sink coordinated are in sorted order, then worst case time complexity to find the sink nodes allotted to all the T tiles is O (T × Nlog N). Calculation of center of mass (CM) for each tile can be done in constant time, by performing arithmetic mean of the coordinates of sink terminals. Sorting of T number of CMs can be done in O(T log T) time. Hence, total time requirement in this stage is O(T) +O(T log T)) ≈ O(T log T). During the first stage of global game play, CM of every tile is treated as an individual player. We assumed that for every player, there are only four strategies {SN, SS, SR, SL}. When the game is played, outcome of the game is the trunk of an optimized delay tree, by playing the game with a constant number of iterations. Hence, to connect total T number of CMs, worst case time complexity is $O(T \times 4^T)$. During connecting the sink terminals to the CMs locally in each tile, we assume that each tile contains number of sink terminals sn << N. Each tile contains sn = N/T number of sinks on average. Hence time complexity to play the game locally is, $O(T \times sn \times 4^{sn}) \approx O(T \times (N/T) \times (4)^{N/T}) \approx O(N \times (4)^{N/T})$. Total time complexity to construct obstacle avoiding clock tree is $O(M \times T) + O(T \times N\log N) + O(T \log T) + O(T \times 4^T) + O(T) + O(N \times (4)^{N/T}) \approx O(M \times T) + O(T \times N\log N) + O(T \log T) + O(N \times (4)^{N/T})$. The space complexity of the game theory based routing algorithm is entirely dependent on the number of global players (T), number of obstacles M, number of sink terminals N, and the size of the payoff matrix to store the payoff functions in each iteration. For four strategy players with maximum T players, storage requirement is O(T + T × 4) ≈ O(T). Maintaining data structure for obstacle edge information in T tiles, and sink coordinates require O(T) and O(N) storage respectively. Hence, total space complexity for running the proposed algorithm is approximately O(N) + O(T).

Existence of Nash Equilibrium:

Let us consider the case of ith player, with payoff function Pi. Nash equilibrium is assumed to exist for the set of strategy $s^* = \{s_1^*, s_2^*, \ldots, s_N^*\}$ with Payoff function P_i^*. All the strategy played are combination of displacements in x and y directions. Payoff function P_i is minimum for the strategy set s*, with minimum clock skew at the i^{th} player, calculated using Equation (1) and Equation (2). Any alternative combination of N tuple in s will generate new displacement values in x and y directions, leading to different payoff function $P_i(s_1, s_2, \ldots s_N) > P_i^*(s_1^*, s_2^*, \ldots, s_3^*)$. This is true for all the N players, played sequentially, proving the existence of Nash equilibrium.

VIII. EXPERIMENTAL RESULTS

Our proposed algorithm is implemented in C, and experiments are performed on a 2.2GHz. Intel i3 core Linux platform with 4 GB RAM. ISPD 2010 benchmark suite [9] is used as the input to run our algorithm. The ISPD 2010 High Performance Clock Network Synthesis Contest was based on 45nm Technology. They consider clock source at (0, 0) and inverter placed exactly at clock source. The tool should assume inverted signal from clock source, since it will be automatically added by the inverter in the input file. They provide translator to translate input file to output file. For each benchmark, normal voltage and various settings are provided. There is worst LCS unit mentioned in each benchmark. For each inverter type, input and output capacitance is provided for total capacitance calculation. Table 1 shows a comparative study of local clock skew within LCS distance specified in the benchmark [9], with the best values obtained in [9]. Minimum skew in the sink terminals in our case is cited to be zero ps, whereas maximum clock skew deviates from the best result in [9] from 44% to 70%. CPU execution time in our algorithm is much less than that in [9]. Table 2 represents clock skew values after complete Rectilinear Clock tree construction and measuring clock skew far away from LCS distance. The tree constructed is called global clock tree, which is constructed following the game theoretic approach described in Section VI. Source terminal is considered to be located at the lower left corner of the layout, from where clock signal is distributed to all the sink terminals. Tiles are generated for global clock tree construction to compensate extra clock skew encountered by the distant sink terminals. Strategy is played in each iteration of the game to achieve the minimal skew at the corresponding sink terminal considered as the player. In ISPD contest [9], authors provide with the best results for local skew. They did not consider the construction of global clock skew to equalize delay at all the sink terminals. The authors in [9] used ngspice simulator to compute delay and clock skew. However, in our work Elmore delay model is used to account for both the local and global clock skew. It is observed from Table 2 that optimal payoff after several iteration of a game delivers good and minimized skew value for global clock tree as well. However, in this phase of global clock tree construction, exact equalization of delay is not possible, as it leads to incorporation of bend wires and more added Steiner points, and hence increases in ultimate path delay. A future directive would be to consider buffer insertion at the improvement of less wire bend and number of Steiner points to equalize delay at global sink terminals.

Table 1: Comparative Study of Local Clock Skew with the Results in [9]

Benchmark Name	# Sinks	# Blockages	Specified LCS (ps)	Best LCS (ps) [9]		CPU (sec) [9]	LCS ours (ps)		CPU Exec. Time (sec)
				Min Skew	Max Skew		Min Skew	Max Skew	

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ispd10cns01	1107	4	7.5	3.19	10.11	12015	0.00	282.89	7.58
ispd10cns02	2249	1	7.5	3.45	9.24	25006	0.00	422.22	8.53
ispd10cns03	1200	2	4.9	1.6	5.04	8	0.00	22.19	6.66
ispd10cns04	1845	2	7.5	2.04	6.06	6075	0.00	9.88	7.6
ispd10cns05	1016	1	7.5	1.51	6.51	7	0.00	39.05	6.74
ispd10cns06	981	0	7.5	3.43	13.98	1258	0.00	7.12	6.62
ispd10cns07	1915	0	7.5	2.02	5.61	2351	0.00	20.01	6.79
ispd10cns08	1134	0	7.5	3.76	9.05	7	0.00	17.44	7.89

Table 2: Experimental Results for Clock Skew Values beyond LCS Distance

Benchmark Name	No. of Tiles Generated (T)	Global Clock Skew (ns)	
		Min skew	Max skew
ispd10cns01	196	0.00283	0.00395
ispd10cns02	264	0.00423	0.00871
ispd10cns03	6	0.00023	0.00058
ispd10cns04	20	0.00010	0.00025
ispd10cns05	20	0.00039	0.00066
ispd10cns06	8	0.00007	0.00025
ispd10cns07	15	0.00020	0.00047
ispd10cns08	12	0.00017	0.00032

IX. CONCLUSION

Interconnect delay optimization is a major performance metric for successful design and yield of a VLSI chip. In this paper, we proposed a delay equalization technique for rectilinear clock tree routing, in presence of rectangular obstacles. Clock skew minimization is performed adopting a non cooperative game theory approach. Clock skew optimized rectilinear delay tree is constructed on the basis of a top down approach. Initial phase starts with dividing the state space into number of tiles, and performing global clock skew optimization. Next, clock skew in each sink is minimized performing routing in each tile. A detail complexity analysis in Section VII shows that time complexity of our algorithm is dominated by $O(T \times NlogN) \approx O(NlogN)$, where T is the number of tiles, and N is the number of sink terminals. Experimental results show that our algorithm is capable of minimizing clock skew within a proposed bound. Crosstalk and noise are the other two important performance metrics, deciding the signal integrity and functionality of a chip. In future, present work may be extended for crosstalk and noise analysis. Buffer insertion and gate sizing for zero skew clock design may also be a possible future directive.

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