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Performance of Improved Multiplier Based On Low-Cost Low-Power Bypassing Technique

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Abstract: - It is well known that multipliers consume most of the power in DSP computations. Hence, it is very important for modern DSP systems to develop low-power multipliers to reduce the power dissipation. This paper presents 8 ×8 and 16×16 low power row and column bypass multiplier design. The switching activity of the component used in the design depends on the input bit coefficient. This means if the input bit coefficient is zero, corresponding row or column of adders need not be activated. If multiplicand contains more zeros, higher power reduction can be achieved. To reduce the switching activity is to shut down the idle part of the circuit, which is not in operating condition. Further low power adder structure reduces the switching activity. If we can reduce the power consumption of the multiplier block, then we can reduce the power consumption of various digital signal processing chips and communication system.

Index Terms—**multiplier, power reduction, switching activity, signal processing.**

I. INTRODUCTION

First, we denote the two 8-bit magnitudes to be multiplied as *A*7-0 and *B*7-0 and the 16-bit product that results as *P*15-0. We can partition *A* and *B* into two 4-bit groups, *A*7-4, *A*3-0, *B*7-4, *B*3-0, and form their 16-bit product as a sum of several 8-bit products:

$A = A_{7-4}\ A_{3-0}$
$\times\quad B = B_{7-4}\ B_{3-0}$

$A_{3-0} \times B_{3-0} = PP_0$
$A_{7-1} \times B_{3-0} = PP_1$
$A_{3-0} \times B_{7-1} = PP_2$
$A_{7-1} \times B_{7-1} = PP_3$

FIG NO.1 Braun Multiplier

$P_{15-12}\ \ P_{11-8}\ \ P_{7-1}\ \ P_{3-0}$

To see how this works, let's examine the multiplication of the 8-bit binary numbers 111100102 and 100011002. These correspond to the decimal numbers 242 and 140, respectively.

```
      1111 0010
   ×  1000 1100
   ---------------
      0001 1000      (0010×1100)
   1011 0100         (1111×1100)
   0001 0000         (0010×1000)
0111 1000            (1111×1000)
---------------
1000 0100 0101 1000
```

As a check, we see that 242 * 140 = 33880, which is equal to 1000010001011000_2.

II. BASIC PARALLEL ARRAY MULTIPLIER STRUCTURE

The multiplication is an essential arithmetic operation for common DSP and communication application, such as filtering and FFT. For the multiplication of two unsigned n-bit numbers, the multiplicand, $A=a_{n-1}\ a_{n-2},\ldots\ldots,\ a_0$ and the multiplier ,$B=b_{n-1},b_{n-2},\ldots\ldots,b_0$ the product $P=P_{2n-1},P_{2n-2},\ldots\ldots P_0$ can be represented as the following equation:

$$P = P_0\ P_1\ \ldots\ P_{2n-1} = \sum (a_i b_j) 2^{(i+j)} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots (2).$$

To achieve the high-performance demand in DSP Applications, the structure of a parallel array multiplier is widely used and a typical array Implementation of such a Parallel multiplier is known as theBraun's design as shown in fig.1.

```
                                A7 A6 A5 A4 A3 A2 A1 A0
                              XB7 B6 B5 B4 B3 B2 B1 B0
-------------------------------------------------------
A7.B0 A6.B0 A5.B0 A4.B0 A3.B0 A2.B0 A1.B0 A0.B0
+ A7.B1 A6.B1 A5.B1 A4.B1 A3.B1 A2.B1 A1.B1 A0.B1
+ A7.B2 A6.B2 A5.B2 A4.B2 A3.B2 A2.B2 A1.B2 A0.B2
+ A7.B3 A6.B3 A5.B3 A4.B3 A3.B3 A2.B3 A1.B3 A0.B3
+ A7.B4 A6.B4 A5.B4 A4.B4 A3.B4 A2.B4 A1.B4 A0.B4
+ A7.B5 A6.B5 A5.B5 A4.B5 A3.B5 A2.B5 A1.B5 A0.B5
+ A7.B6 A6.B6 A5.B6 A4.B6 A3.B6 A2.B6 A1.B6 A0.B6
+A7.B7 A6.B7 A5.B7 A4.B7 A3.B7 A2.B7 A1.B7 A0.B7-----------------------------------
P15 P14P13 P12 P11 P10P9P8 P7 P6P5P4P3P2 P1 P0
```

FIG NO. 2 Multiplication of two-8 bit nos.

Based on the 4×4 multiplier design architecture only the next stages are considered and the 8×8 and 16×16 architecture are taken into consideration.

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III. ROW BYPASSING AND COLUMN BYPASSINGBASED MULTIPLIER DESIGN

Turning of some rows or columns or both in the multiplier or multiplicand or both bits are zero is known as bypassing with reference to the multiplier. The row bypassing technique is based on the number of zeros in the multiplier bits. In order to save the power in the multiplier operation some of the row of adders in the array are made disabled during operation. Following fig.3 shows the structure of modified FA cell used for minimizing power dissipation used for the design implementation of 8×8 and 16×16 multipliers. For low-power row bypassing multiplier, the addition operation in the j-th row can be bypassed for the power reduction if the bit,bj, in the multiplier is 0,i.e. partial products are zero.

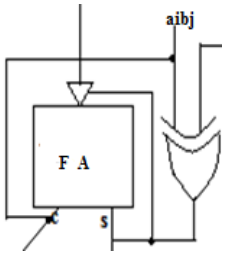

Fig no. 3 Modified FA cell.

The operations in the column bypassing can be disabled if the corresponding bit in the multiplicand is zero, to save the power and this technique is totally dependent on the multiplicand bits. Modification is done in the cell circuit which is simpler than FA used in row bypassing as shown in fig.4.

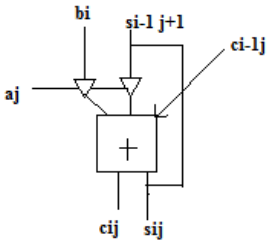

Fig no. 4 Cell circuit for column bypassing

IV. RESULTS

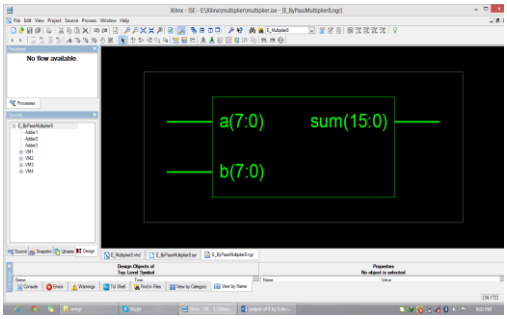

Fig No.5 RTL Schematic output of 8 × 8 Multiplier is as shown in the Xilinx in which the two inputs of 8-bits and output of 16-bits is observed.

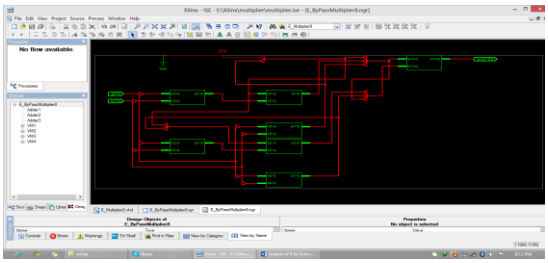

Fig No.6 Zooming RTL Schematic view Output of 8 × 8 Multiplier of above fig, in which half adder and full adder component are seen on the Xilinx.

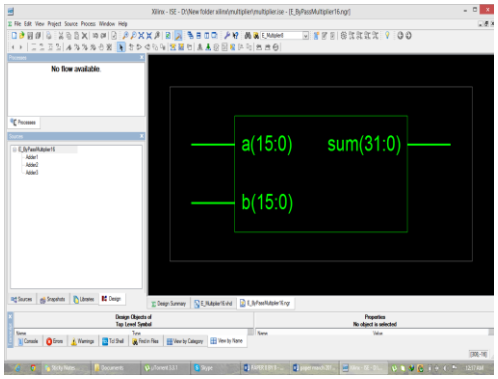

Fig No.7 RTL Schematic output of 16 × 16 Multiplier is as shown in the Xilinx in which the two inputs of 8-bits and output of 32-bits is observed.

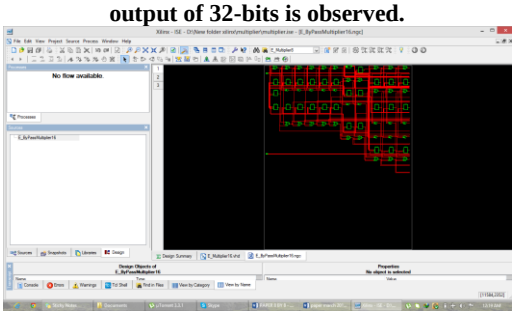

Fig No.8 Zooming RTL Schematic view Output of 16 × 16 Multiplier of above fig, in which half adder and full adder component are seen on the Xilinx.

VI. CONCLUSION

Based on the simplification of the addition of operation, the proposed low-cost low-power improved bypassing results based multiplier design using 8-bits and 16-bits is as shown in the below table with respect to power dissipation and area overhead in transistors:

	8×8 Multiplier	16×16 Multiplier
Braun design [1]	1840 (100.0%)	8032 (100.0%)
[2]	2952 (160.4%)	12808 (159.5%)
[3]	2470 (134.2%)	10822 (134.7%)
[4]	3584(194.8%)	16272 (202.6%)
[5]	2428(132.0%)	10972 (136.6%)
[6]	1552(84.3%)	6688 (83.3%)
Our design [7]	376 (20.44%)	1520 (18.93%)

Table No.1 Area overhead in Transistors

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	8×8 Multiplier	16×16 Multiplier
Braun design [1]	3.45 (100.0%)	14.31 (100.0%)
[2]	3.77 (109.3%)	15.52 (108.5%)
[3]	3.17 (91.9%)	13.04 (91.1%)
[4]	4.01(116.2%)	16.94 (118.4%)
[5]	2.75(79.7%)	11.42 (79.8%)
[6]	2.43(70.4%)	10.03 (70.1%)
Our design [7]	1.78(48.40%)	5.15 (64.01%)

Table No.2 Power Dissipation in 8×8 and 16×16 multiplier.

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