ISSN: 2277-3754
ISO 9001:2008 Certified
International Journal of Engineering and Innovative Technology (IJEIT)
Volume 3, Issue 3, September 2013

Nine-Level Cascaded H-Bridge Multilevel Inverter

Divya Subramanian, Rebiya Rasheed

Abstract* —The multilevel inverter utilization have been increased since the last decade. These new type of inverters are suitable in various high voltage & high power application due to their ability to synthesize waveforms with better harmonic spectrum and faithful output.. This paper presents a multilevel inverter configuration which is designed by insertion of a bidirectional switch between capacitive voltage sources and a conventional H-bridge module. The modified inverter can produce a better sinusoidal waveform by increasing the number of output voltage levels. By serial connection of two modified H-bridge modules, it is possible to produce 9 output voltage levels including zero. Multicarrier phase-shifted pulse-width modulation method is used to achieve balanced power distribution among the power cells. The analysis of the output voltage harmonics is carried out. From the results, the proposed inverter provides higher output quality with relatively lower power loss as compared to the other conventional inverters with the same output quality.

***Index Terms*— Cascaded H-bridge multilevel inverter (CHB), multicarrier pulse-width modulation, phase shifted modulation, total harmonic distortion (THD).**

I. INTRODUCTION

Multilevel power conversion has become increasingly popular in recent years due to advantages of high power quality waveforms, low electromagnetic compatibility (EMC) concerns, low switching losses, and high-voltage capability. However, it increases the number of switching devices and other components, which results in an increase of complexity problems and system cost. There are different types of multilevel circuits involved. The first topology introduced was the series H-bridge design. This was followed by the diode clamped converter, which utilized a bank of series capacitors. A later invention detailed the flying capacitor design in which the capacitors were floating rather than series-connected. Another multilevel design involves parallel connection of inverter phases through inter-phase reactors. In this design, the semiconductors block the entire dc voltage, but share the load current. Several combinational designs have also emerged some involving cascading the fundamental topologies. These designs can create higher power quality for a given number of semiconductor devices than the fundamental topologies alone due to a multiplying effect of the number of levels. The multilevel inverters are mainly classified as diode clamped, Flying capacitor inverter and cascaded multilevel inverter. The cascaded multilevel control method is very easy when compare to other multilevel inverter because it doesn't require any clamping diode and flying capacitor. In this paper, we are using a new topology of cascaded H-bridge multilevel inverter for producing nine output voltage levels and for that we are using multicarrier modulation technique.

II. NINE-LEVEL CASCADED H-BRIDGE MULTILEVEL INVERTER

The main disadvantage of the conventional cascaded H-bridge [5] is that when the voltage level increases, the number of semiconductor switches increases and also the source required increases. In order to overcome this introduced a new topology of cascaded H-bridge. The main advantage of this topology is that the number of switches required is reduced and also the number of sources. Figure 1 shows the new cascaded five level H-bridge multilevel inverter [6]. It has additional one bidirectional switch connected between the first leg of the H-bridge and the capacitor midpoint, enabling five output voltage levels.

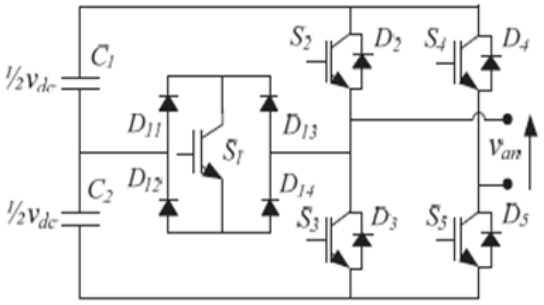

Fig 1. Five level cascaded H-bridge multilevel inverter

It has five output voltage levels ie V_{dc}, $V_{dc}/2$, 0, $-V_{dc}/2$, $-V_{dc}$. For getting the output voltage V_{dc} the switches S_2S_5 need to be turned on. Similarly for output voltage $V_{dc}/2$ switches S_1S_5 need to be turned on, for 0 either S_3S_5 or S_2S_4 need to be turned on; for - $V_{dc}/2$ switches S_1S_4 need to be turned on; for - V_{dc} switches S_3S_4 need to be turned on. The switch combinations are shown in table 1.

Table -1: Five- level cascaded h-bridge output voltage

S_1	S_2	S_3	S_4	S_5	v_{an}
0	1	0	0	1	v_{dc}
1	0	0	0	1	$\frac{1}{2}v_{dc}$
0	0 or 1	1 or 0	0 or 1	1 or 0	0
1	0	0	1	0	$-\frac{1}{2}v_{dc}$
0	0	1	1	0	$-v_{dc}$

(Switch ON = 1, Switch OFF = 0)

ISSN: 2277-3754
ISO 9001:2008 Certified
International Journal of Engineering and Innovative Technology (IJEIT)
Volume 3, Issue 3, September 2013

In the circuit shown in fig 1, single H-bridge module is capable of producing five level output voltage. Each inverter module is capable of producing 2E, E, 0, -E, -2E. That means by using two bridges 9 level output voltage is produced. The total output voltage is sum of the outputs of the inverter modules and the nine voltage levels are 4E, 3E, 2E, E, 0, -E, -2E, -3E, -4E. The advantages of this proposed circuit is number of switches are reduced. The cost and complexity is less in this circuit. To synthesize nine output voltage levels, it employs two independent dc voltage sources of 2*E* which are divided into two input sources *E* in order to secure an additional dc voltage source of *E*. The inverter module having a bidirectional switch produces 5-levels of output voltage (-2*E*, -*E*, 0, *E*, 2*E*) by controlling of the switches. Since every output terminal of the inverter module is connected in series, the output voltage becomes the sum of the terminal voltages of each inverter. The circuit for nine level cascaded H-bridges is shown in figure 2, the gating signals for the inverter is generated by using multicarrier modulation.

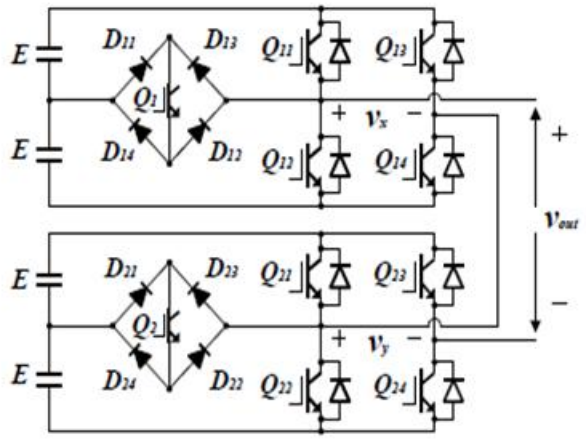

Fig 2. Nine level cascaded H-bridge multilevel inverter

III. PWM MODULATION

In this inverter, the sinusoidal pulse width modulation is going to use. In the Sinusoidal pulse width modulation scheme, as the switch is turned on and off several times during each half-cycle, the width of the pulses is varied to change the output voltage. Lower order harmonics can be eliminated or reduced by selecting the type of modulation for the pulse widths and the number of pulses per half-cycle. Higher order harmonics may increase, but these are of concern because they can be eliminated easily by filters. The SPWM aims at generating a sinusoidal inverter output voltage without low-order harmonics. This is possible if the sampling frequency is high compared to the fundamental output frequency of the inverter. The modulation index, *M* of the proposed multilevel inverter is defined by,

$$M = \tfrac{1}{2} (V_{ref} / V_{cr}) \qquad (1)$$

where V_{ref} is the amplitude of the voltage reference and V_{cr} is the amplitude of the carrier signal.

Multicarrier phase-shifted PWM (CPS-PWM) [7] modulation is used to generate the PWM signals. The amplitude and frequency of all triangular carriers are the same as well as the phase shifts between adjacent carriers. Depending on the number of cells, the carrier phase shift for each cell, $\theta_{cr,n}$ can be obtained from,

$$\theta_{cr,n} = 2\pi(n-1)/N_c \text{ , } n= 1,2,\ldots\ldots N_c \qquad (2)$$

For signal generation in each cell, two voltage references and one carrier signal are used. V_{ref} is defined by

$$V_{ref} = M \sin \omega t \qquad (3)$$

$$V_{ref1} = | V_{ref} | \qquad (4)$$

$$V_{ref2} = | V_{ref} - 1/2 | \qquad (5)$$

Both references are identical but displaced by an offset equal to the carrier's amplitude which is ½. When the voltage reference is between 0<*vref*≤½, *vref1* is compared with the triangular carrier and alternately switches *S1* and *S3* while maintaining *S5* in the ON state to produce either ½*vdc* or 0. Whereas, when the reference is between ½<*vref*≤1, *vref2* is used and alternately switches *S1* and *S2* while maintaining *S5* in the ON state to produce either ½*vdc* or *vdc*. As for the reference between –½<*vref*≤0, *vref1* is used for comparison which alternately switches *S1* and *S2* while maintaining *S4* in the ON state to produce either –½*vdc* or 0. For a voltage reference between –1<*vref*≤–½, *vref2* is compared with the carrier to produce either –½*vdc* or –*vdc* alternately switches *S1* and *S3*, maintaining *S4* in the ON state. It is noted that two switches, *S4* and *S5*, only operate in each reference half cycle. This implies that both switches operate at the fundamental frequency while the others operate close to the carrier frequency. This allows the dc voltage to be switched at a low frequency so as to reduce the switching losses. Fig.3 shows the modulation scheme used for the proposed two-cell configuration and Fig. 4 shows a detail block diagram for generating the PWM signals.

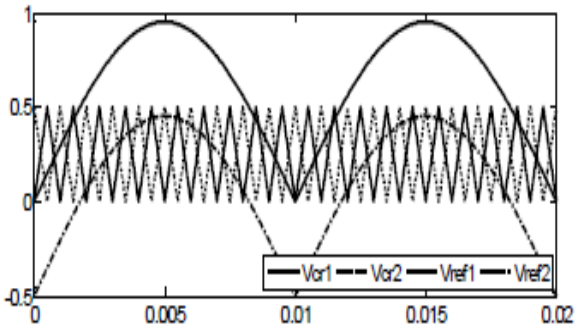

Fig 3. . Multicarrier phase-shifted PWM for two-cell configuration

ISSN: 2277-3754
ISO 9001:2008 Certified
International Journal of Engineering and Innovative Technology (IJEIT)
Volume 3, Issue 3, September 2013

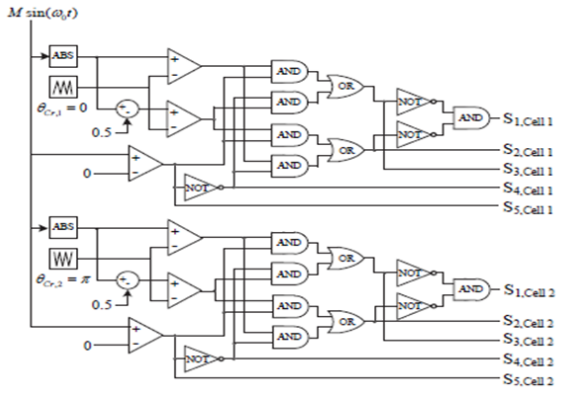

Fig 4. PWM signal generation with multicarrier phase-shifted modulation

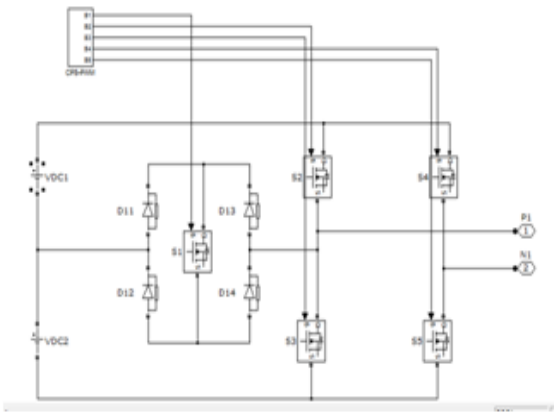

Fig 7. Circuit of cell 2

IV. SIMULATION AND RESULTS

The simulation model was designed using MATLAB/Simulink Software. The gating signals for the inverter are generated by using multicarrier modulation technique. The circuit was simulated with RL load.

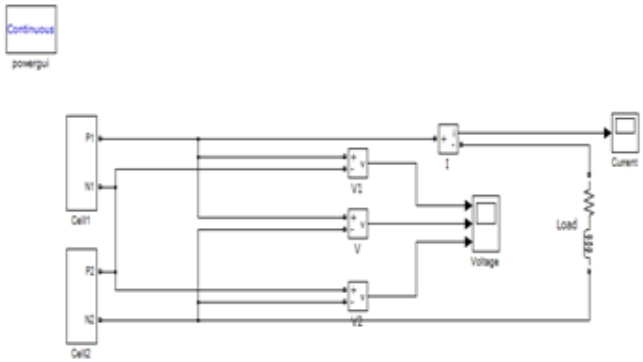

Fig 5 Circuit for Nine level Cascaded H-bidge Multilevel Inverter.

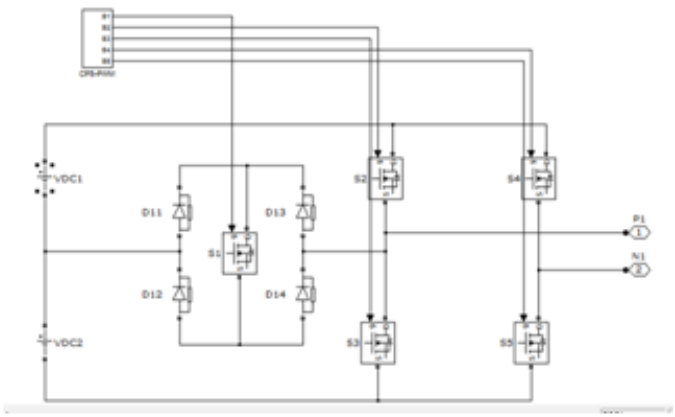

Fig 6 Circuit of cell 1.

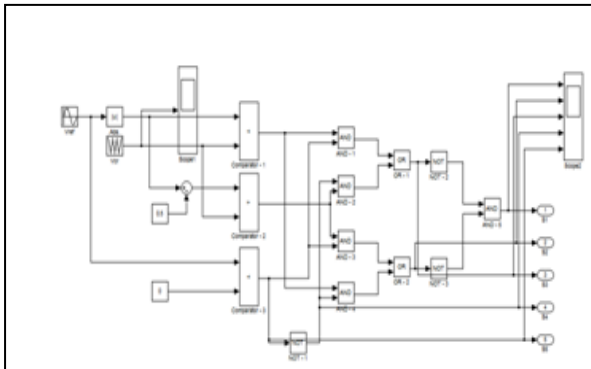

Fig 8 . Circuit for PWM signal generation

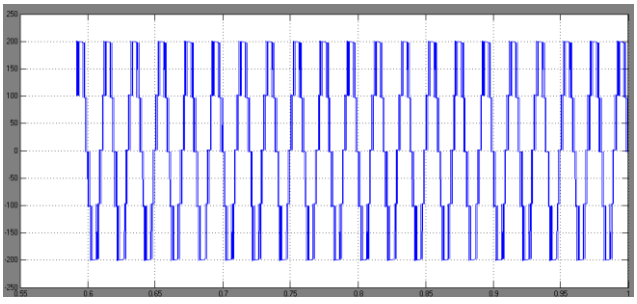

Fig 9. Output voltage waveform for cell 1

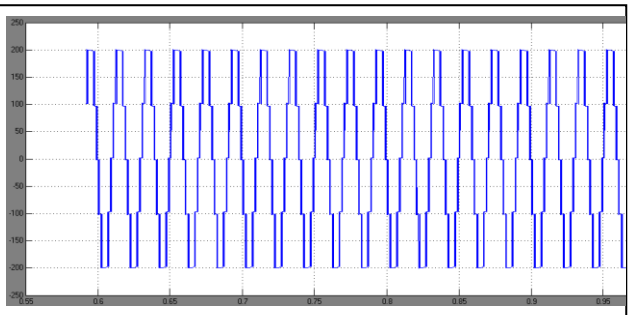

Fig 10 . Output voltage waveform for cell 2

ISSN: 2277-3754
ISO 9001:2008 Certified
International Journal of Engineering and Innovative Technology (IJEIT)
Volume 3, Issue 3, September 2013

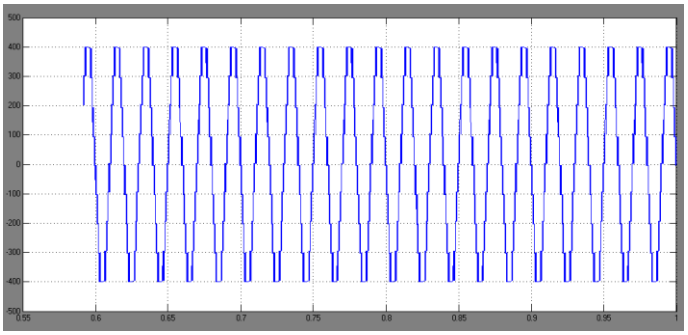

Fig 11. . Output voltage waveform

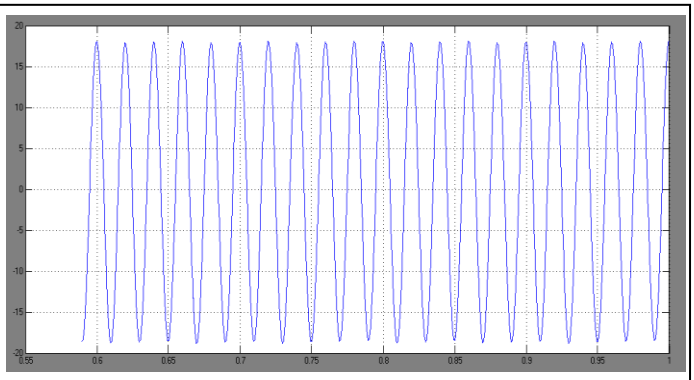

Fig 12. . Output current waveform

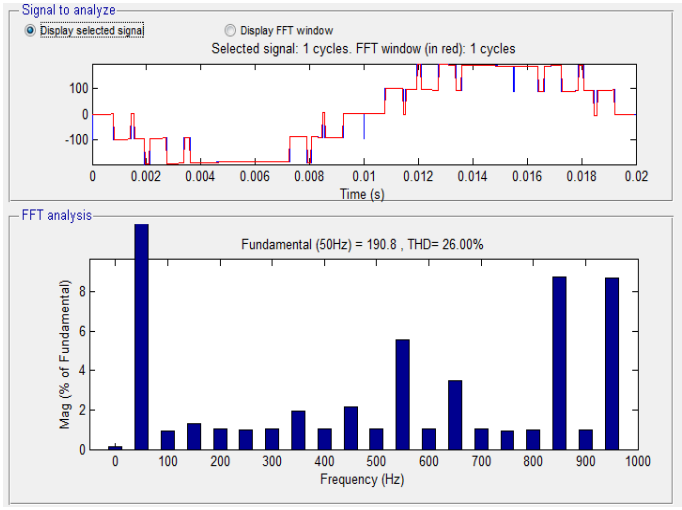

Fig 13. Five level cascaded H-bridge multilevel inverter with multicarrier modulation , THD=26.00%.

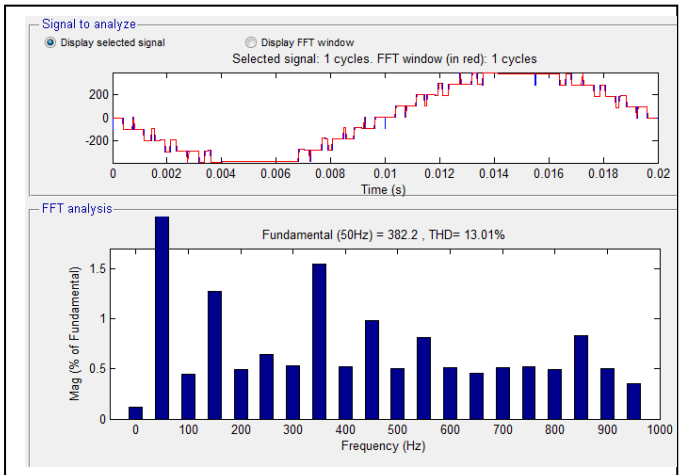

Fig 14. Nine level cascaded H-bridge multilevel inverter with multicarrier modulation, THD=13.01%.

V.CONCLUSION

Multilevel inverters have become an effective and practical solution for increasing power and reducing harmonics of ac waveforms. This project deals with the design and implementation of single-phase nine-level Cascaded H-bridge multilevel inverter for RL load with multicarrier phase-shifted PWM modulation method. The simulation of 9-level cascaded H-bridge is done. Along with it, it's harmonic analysis was done. The simulation results shows that the developed nine-level Cascaded H-bridge Multilevel inverter has many merits such as reduce number of switches, lower EMI, less harmonic distortion and the THD obtained is 13.01%.

ACKNOWLEDGMENT

Fore mostly, I would like to express my sincere gratitude to our Principal: Dr K. S.M Panicker, for his guidance. I am also thankful to our HOD Dr.Pailo Paul for imparting fundamental idea, which helped me a lot for my project. I am extremely thankful to my guide Mrs.Rebiya Rasheed for her guidance and suggestions, I would also like to thank all my teachers and my husband Mr.Veneesh C.S who gave their full support and encouragement for doing this project. I owe my deepest gratitude to them

REFERENCES

[1] Nasrudin Abd. Rahim, Mohamad Fathi Mohamad Elias, Wooi Ping Hew, IEEE transaction. Industry Electronics, "Design of filter to reduce harmonic distortion in industrial power system", Vol. 60, No :8, 2943-2956, August 2013.

[2] J. Selvaraj and N. A. Rahim, "Multilevel Inverter For Grid-Connected PV System Employing Digital PI Controller," IEEE Trans. Ind.Electron., vol. 56, pp. 149-158, 2009.

[3] Naderi and A. Rahmati, "Phase-Shifted Carrier PWM Technique for General Cascaded Inverters," IEEE Trans. Power Electron., vol. 23, pp. 1257-1269, 2008.

ISSN: 2277-3754
ISO 9001:2008 Certified
International Journal of Engineering and Innovative Technology (IJEIT)
Volume 3, Issue 3, September 2013

[4] J. Rodriguez, J.-S. Lai, and F. Z. Peng, ―Multilevel inverters: A survey of topologies, controls, and applications,‖ IEEE Trans. Ind. Electron., vol. 49, no. 4, pp. 724–738, Aug. 2002.

[5] M. Malinowski, K. Gopakumar, J. Rodriguez, and M. A. Pérez, ―A Survey on cascaded multilevel inverters,‖ IEEE Trans. Ind. Electron., vol. 57, no. 7, pp. 2197-2206, July 2010.

[6] S. J. Park, F. S. Kang, M. H. Lee, and C. U. Kim, ―A new single-phase five-level PWM inverter employing a deadbeat control scheme,‖ IEEE Trans. Power Electron., vol. 18, no. 18, pp. 831–843, May 2003.

[7] N. A. Rahim, and J. Selvaraj, ―Multistring five-level inverter with novel PWM control scheme for PV application,‖ IEEE Trans. Ind. Electron., vol. 57, no. 6, pp. 2111-2123, June 2010.