ISSN: 2277-3754
ISO 9001:2008 Certified
International Journal of Engineering and Innovative Technology (IJEIT)
Volume 3, Issue 2, August 2013

MMC Based HVDC System

Harikrishnan K, Rinku scaria

Abstract*— This paper presents modelling and simulation of a high voltage HVDC transmission system. Instead of using conventional voltage source converter Modular multilevel converter is used in this system this paper presents a generalized mathematical model for MMC in realistic HVDC applications. In the model, as the number of levels in the converter increases, consequently, the number of redundant switching states increases. This thesis has provided a dc capacitor voltage balancing method for multi-level converters that in each sample of time selects the proper redundant switching states to solve the voltage drifting problem at the dc capacitors. From the simulation results, it is observed that the developed method is able to equalize the dc side capacitor voltages without using any additional power circuits. Based on the simulations, it is shown that among all the switching strategies, the provided balancing method leads to better capacitor voltage balancing at the side and also better harmonic spectrum for output voltage at the ac side. The aim of this project was the analysis of a Modular Multilevel Converter (MMC) for HVDC applications. The modelling of control scheme of The proposed system is simulated using MATLAB/SIMULINK software.

***Index Terms*—HVDC, VSC (voltage source converter), MMC (modular multilevel converter).**

I. INTRODUCTION

The development of new technologies and devices during the 20th century enhanced the interest in electric power systems. Modern civilization based his operation on an increasing energy demand and on the substitutions of human activities with complex and sophisticated machines; thus, studies on electric power generation and conversion devices become every day more and more important. The recent attention in environment protection and preservation increased the interest in electrical power generation from renewable sources: wind power systems and solar systems are diffusing and are supposed to occupy an increasingly important role in world-wide energy production in coming years. Not only house utilities, but industrial applications and even the electrical network requirements display the importance that energy supply and control will have in the future researches. As a consequence, power conversion and secondly control is required to be reliable, safe and available in order to accomplish all requirements, both from users and legal regulations, and to reduce the environmental impact. Voltage Source Converter (VSC) technology is becoming common in high-voltage direct current (HVDC) transmission systems (especially transmission of offshore wind power, among others). HVDC transmission technology is an important and efficient possibility to transmit high powers over long distances.

II. MODULAR MULTILEVEL CONVERTER

Modular multilevel converter is a type of voltage source converter which converts ac voltage into dc voltage. The modular multilevel converter (MMC) was first introduced in 2001 [3]. This converter is an emerging cascaded multilevel converter with common dc bus, and considered suitable for VSC-HVDC transmission [4]–[10]. MMC is well scalable to high-voltage levels of power transmission based on cascade connection of multiple sub modules (SMs) per arm [4], which also means a high number of output voltage levels (e.g., “Trans Bay Cable” Project is at 400 kV dc voltage, and about 200 SMs per arm [6]). The high number of voltage levels provides high quality output voltage with low common-mode voltage, also known as zero-sequence voltage in a three-phase ac system [11]. Thus, only small or even no filters are required. Another advantage of the high-level number is that low switching frequency modulation scheme can be adopted to reduce semiconductor switching losses.

III. DESCRIPTION AND PRINCIPLE OF OPERATION OF MMC

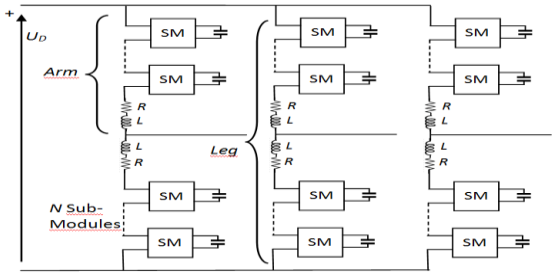

Fig .1 - Schematic of a three-phase Modular Multi-level Converter

The typical structure of a MMC is shown in Fig.1, and the configuration of a Sub-Module (SM) is given in Fig.2. Each SM is a simple chopper cell composed of two IGBT switches (T1 and T2), two anti-parallel diodes (D1 and D2) and a capacitor C. Each phase leg of the converter has two arms, each one constituted by a number N of SMs. In each arm there is also a small inductor to compensate for the voltage difference between upper and lower arms produced when a SM is switched in or out. With reference to the SM shown in Fig..3, the output voltage U0 is given by,

U0 = Uc if T1 is ON and T2 is OFF
U0 = 0 if T1 is OFF and T2 is ON
Where Uc is the instantaneous capacitor voltage.

The configuration with T1 and T2 both ON should not be considered because it determines a short circuit across the capacitor. Also the configuration with T1 and T2 both OFF is not useful as it produces different output voltages depending

ISSN: 2277-3754
ISO 9001:2008 Certified
International Journal of Engineering and Innovative Technology (IJEIT)
Volume 3, Issue 2, August 2013

on the current direction. Fig. 4 shows the current flows in both useful states. In a MMC the number of steps of the output voltage is related to the number of series connected SMs. In order to show how the voltage levels are generated, in the following, reference is made to the simple three level MMC configurations shown in Fig 4.

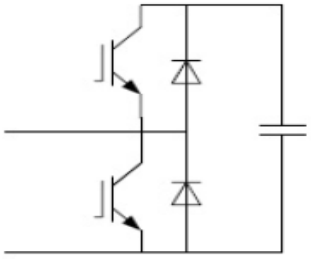

Fig .2 – Chopper cell of a Sub-Module

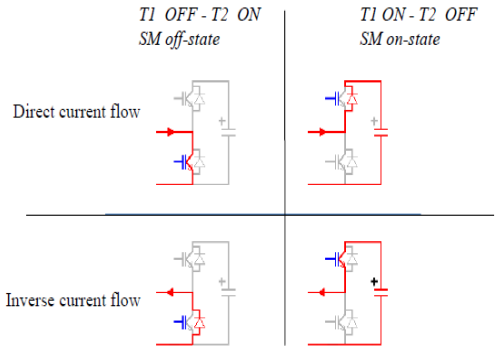

Fig .3 - States of SM and current paths

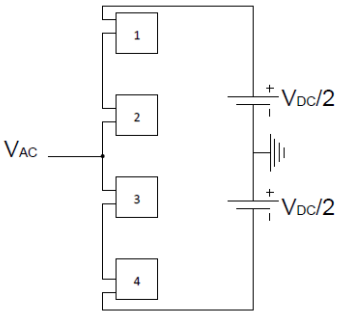

Fig .4 - Schematic of one phase of Three-Level Converter

In this case, in order to get the positive output, +*UD/2*, the two upper SMs 1 and 2 are bypassed. Accordingly, for the negative output, - *UD/2*, the two lower SMs 3 and 4 are bypassed. The zero state can be obtained through two possible switch configurations. The first one is when the two SMs in the middle of a leg (2 and 3) are bypassed, and the second one is when the end SMs of a leg (1 and 4) is bypassed. It has to be noted that the current flows through the SMS that are not by passed determining the charging or discharging of the capacitors depending on the current direction. Therefore, in order to keep the capacitor voltages balanced, both zero states must be used alternatively. The voltage waveform generated by the three level converters is shown in Fig2.5.

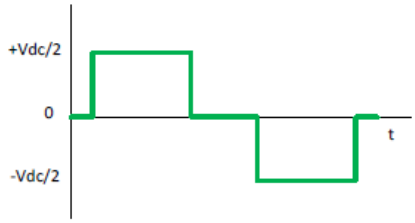

Fig .5 - Voltage waveform of a Three-Level Converter

The principle of operation can be extended to any multi-level configuration as the one represented in Fig. 2.6.

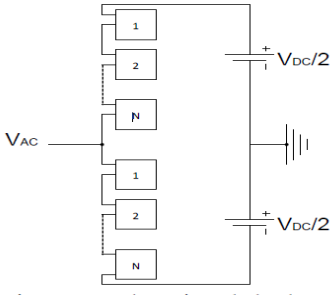

Fig .6 - Schematic of one phase of Multi-Level Converter

In this type of inverter, the only states that have no redundant configurations are the two states that generate the maximum positive and negative voltages, + *UD/2* and –*UD/2*. For generating the other levels, in general there are several possible switching configurations that can be selected in order to keep the capacitor voltages balanced. In MMC of Fig. 6, the switching sequence is controlled so that at each instant only N SMs (i.e. half of the 2N SMs of a phase leg) are in the on-state. As an example, if at a given instant in the upper arm SMs from 2 to N are in the on-state, in the lower arm only one SM will be in on-state. It is clear that there are several possible switching configurations. Equal voltage sharing among the capacitor of each arm can be achieved by a selection algorithm of inserted or bypassed SMs during each sampling period of the control system. A typical voltage waveform of a multi-level converter is shown in Fig . 7

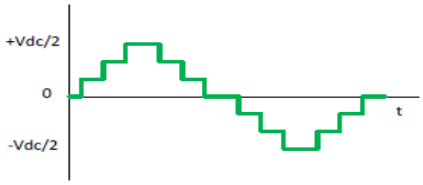

Fig .7 - Voltage waveform of a Multi-Level Converter

IV. MMC MODEL

The typical structure of an MMC, shown in Fig. 1, can be summarized into 3 levels:

I. sub-modules SM (the lower level, usually Chopper cells)
II. arm (second level of the converter, half of the leg-phase)
III. leg (can be considered one phase)

ISSN: 2277-3754
ISO 9001:2008 Certified
International Journal of Engineering and Innovative Technology (IJEIT)
Volume 3, Issue 2, August 2013

If a two-level control structure is considered, for instance a Master-Slave structure, lower level of control is assigned to sub-models (level I), instead upper level of control deals with arm-leg voltage and currents control (level II, III). It is assumed that a lower level control for the sub-modules is present ensuring that all capacitors are equally charged. As suggested in [13], most of existing investigations and simulations are based on switched or discrete models. However, discrete models have two main disadvantages:

a) Discrete models do not allow an analytical approach to model the converter and to design the control system; b) Numerical solution of complex converter configurations using a high number of SMs requires considerable simulation time. A continuous model can overcome these disadvantages. Therefore, to clearly understand the operation of this converter it is necessary to write the voltage-current equations and to determine a continuous model suitable to design a control scheme. In the following, an analysis is carried out with the aim to control the upper and lower arm voltages, using the continuous model presented in [8], that considers only one converter phase and is based on time-variable capacitors.

V. MATHEMATICAL MODEL OF MMC

Considering a converter with N sub-modules per arm, each arm can be controlled with an insertion index (modulation index) n(t), where n(t)=0 means that all sub-modules in the arm are by-passed, on the other side n(t)=1 means that all the sub-modules in the arm are inserted. Ideal capacitance of the arm should be:

$$C^{arm} = \frac{C}{N} \tag{3.2.1}$$

$$C^{m} = \frac{C^{arm}}{n(t)} \tag{3.2.2}$$

Where the m apex means the number of the arm (for instance, in a three-phase converter m=1,2,3,..,6). It would be possible to have a full representation of the MMC converter, including operation of each sub-module, but this approach tends to be fairly complicated and not easy to be used as a base for control schemes development. A simpler way would be to consider a continuous model, but 2 important assumptions are necessary in order to develop this approach:

1. the switching frequency is much higher than the frequency of the output voltage
2. The resolution of the output voltage is small, compared to the amplitude of the output voltage (i.e. high number of sub-modules)

Assuming 1 and 2, it's possible to create a continuous model which represents the overall operation of the converter, neglecting the single sub-modules behavior: this type of model is suitable for control system design and makes it possible to focus on the energy stored in the converter and its balance between arms. The simplified model is shown in Fig. 8

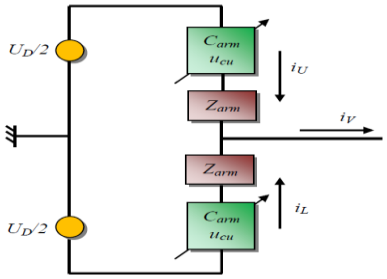

Fig 8 - Simplified Circuit Used for the Analysis

Again, apex m represent the arm, n(t) is the insertion index, instead ucΣ(t) is the sum of all capacitance voltage in the m arm. Then equations (3.2.1) and (3.2.2) follow

$$u_c^m = n(t)\sum u_c(t) \tag{3.2.1}$$

$$\frac{d\sum u_c(t)}{dt} = \frac{i(t)}{C^m} \quad \text{with} \quad C^m = \frac{C^{arm}}{n(t)} \tag{3.2.2}$$

With reference to Fig 9, where only one phase is considered, it is possible to write a set of equations for currents: currents from upper and lower arms, respectively iU and iL, will constitute the output current iV. the idiff current represents the current that circulates from the phase leg to the DC link (and/or to another phase leg).

$$i_V = i_U + i_L \tag{3.2.3}$$

$$i_{diff} = \frac{i_U - i_L}{2}$$

These equations are representing the ideal condition in which the contributions of upper and lower arms to the output current are equal. The difference current is introduced to consider the possible situation in which the capacitors are not equally charged to the reference value. In this MMC configuration the sum of all capacitor voltages of one arm is assumed to be equal to the DC Voltage uD. Equations (3.2.4) and (3.2.5) are just emphasizing the contributions of upper and lower arms in terms of voltage and current

$$\frac{du_{CU}^{\sum(t)}}{dt} = \frac{n_U i_U}{C^{arm}} \tag{3.2.4}$$

$$\frac{du_{CL}^{\sum(t)}}{dt} = \frac{n_L i_L}{C^{arm}} \tag{3.2.5}$$

With all these equations and the simplified circuit shown in Fig. 9, it is possible to write equations (3.2.6) and (3.2.7) as simple Kirchhoff voltage equations

$$\frac{u_D}{2} - Ri_U - L\frac{di_U}{dt} - n_U u_{CU}^{\Sigma} = u_V \tag{3.2.6}$$

$$-\frac{u_D}{2} - Ri_L - L\frac{di_L}{dt} - n_L u_{CL}^{\Sigma} = u_V \tag{3.2.7}$$

ISSN: 2277-3754
ISO 9001:2008 Certified
International Journal of Engineering and Innovative Technology (IJEIT)
Volume 3, Issue 2, August 2013

Subtracting equation (3.2.7) to (3.2.6), and substituting the following equations

$$\frac{di_U}{dt} - \frac{di_L}{dt} = 2\frac{di_{diff}}{dt} \quad (3.2.8)$$

it is possible to obtain this dynamic equation of the current idiff :

$$\frac{di_{diff}}{dt} = \frac{u_D}{2L} - \frac{R}{L} i_{diff} - \frac{n_U}{2L} u\Sigma_{CU} - \frac{n_L}{2L} u\Sigma_{CL} \quad (3.2.9)$$

From equations (3.2.6) and (3.2.7)substituting iU and iL with the expressions given in (3.2.3) two dynamic equations of upper and lower arm voltages are obtained

$$\frac{du_{CL}^{\Sigma}}{dt} = \frac{n_L}{C^{arm}} i_{diff} - \frac{n_L}{2C^{arm}} i_V \quad (3.2.10)$$

From (3.2.10) it can be noted that with idiff equal to zero, the load current acts in order to unbalance the upper and lower arm voltages. In steady state conditions the load current is changing assuming positive and negative values, then, the time derivative of the arm voltages are also changing, and in ideal conditions the arm voltage should oscillate around a constant mean value. The presence of non idealities and losses may lead the converter to be unstable. As a consequence, it can be concluded that only the presence of a suitable difference current allows the converter to operate correctly. Using (3.2.9) and (3.2.10) a dynamic and continuous model is thus obtained and shown

$$\frac{d}{dt}\begin{bmatrix} i_{diff} \\ u_{CU}^{\Sigma} \\ u_{CL}^{\Sigma} \end{bmatrix} = \begin{bmatrix} \frac{-R}{L} & \frac{-n_U}{2L} & \frac{-n_L}{2L} \\ \frac{n_U}{C^{arm}} & 0 & 0 \\ \frac{n_L}{C^{arm}} & 0 & 0 \end{bmatrix} \begin{bmatrix} i_{diff} \\ u_{CU}^{\Sigma} \\ u_{CL}^{\Sigma} \end{bmatrix} + \begin{bmatrix} \frac{u_D}{2} \\ \frac{n_U i_V}{2C^{arm}} \\ \frac{-n_L i_V}{2C^{arm}} \end{bmatrix}$$

Assuming that a sinusoidal output voltage is desired, the reference signal for modulation is

$$m(t) = \hat{m}\cos(\omega_N t) \quad (3.2.12)$$

And the ideal terminal voltage is given by

$$u_V(t) = \frac{u_D}{2} m(t) \quad (3.2.13)$$

In order to solve the system of equations (3.2.11) the load current should be known. Here, the following alternating current is assumed as the output load current

$$i_V(t) = \hat{i}_V(t)\cos(\omega_N t + \phi) \quad (3.2.14)$$

Where φ is the load phase angle and is arbitrary.
Using the reference signal in (3.2.12) the modulation indices for upper and lower arms can be expressed as

$$n_U(t) = \frac{1 - m(t)}{2} \quad (3.2.15)$$

$$n_L(t) = \frac{1 + m(t)}{2} \quad (3.2.16)$$

It can note that the sum of upper and lower modulation indexes is always equal to 1. As a consequence, assuming the capacitor voltages of all modules equal to the reference value, the sum of the voltages of upper and lower arms is always equal to the DC voltage uD . In real operating conditions the capacitor voltages will not be exactly equal to the reference value and as a result a difference voltage will be present forcing a difference current to flow between the leg and the DC source. A suitable control of this current is crucial for achieving a correct operation of the converter and an equal sharing of the DC voltage among all modules. A possible control strategy is the one based on adding an offset voltage to upper and lower arm voltages uCU and uCL defined trough (3.2.15) and (3.2.16). This offset voltage (udiff) is determined with some criteria aimed to keep the module voltages as close as possible to the reference value or to keep the energy stored in upper and lower capacitors equalized. It will be shown in the next section that udiff will not affect the terminal voltage (as uV is related to the difference between upper and lower arm voltages), but will impact on idiff current instead. The number of levels that can be obtained depends on the assumptions made for the analysis. When assuming a constant DC voltage, actually it is possible to generate output voltages having a number of levels equal to 2N+1, whereas the number of levels must be reduced to N+1 if the DC voltage has to be kept under control by the converter itself. This is the situation that occurs in HVDC systems composed by two MMCs connecting the two ends of a DC cable. In this case there is no DC capacitor between the DC voltage terminals and a DC voltage controller is necessary. In this analysis a constant DC voltage will be assumed as the aim is to develop a strategy for keeping under control the total energy stored in each leg and the unbalance between the energy stored in upper and lower arms.

VI. CONTROL STRATEGY

It is necessary to make an important remark: the equations wrote and discussed in previous section lead to a continuous model, suitable for analysis and understanding of operation principle of the MMC. On the other hand, from the control point of view, these equations are not easy to use: even if it is possible to decouple continuous and alternate component of differential current, in order to properly track references, non-linear couplings make really complex advanced control structures. Neglecting this low pass filter it is possible to consider that input variables are a “square” input for the system: this condition makes more difficult the development

ISSN: 2277-3754
ISO 9001:2008 Certified
International Journal of Engineering and Innovative Technology (IJEIT)
Volume 3, Issue 2, August 2013

of advanced control strategies and the study of complex control strategies. Thus, a different approach in the modeling will be developed in order to simplify the analysis from the control point of view. Two different loops will be implemented, the first one to control the overall energy of the MMC leg, the second to control the balance between upper and lower arms of the phase-leg. The interaction between two loops may lead to instability: because of the non-linear configuration of system equations, it is hard to analyze systems coupling properly (for instance Relative Gain Array analysis). It is however evident that total energy and energy balance interacts dynamically in system operation: in order to make a decoupling, balance of energy loop is tuned in order to be greatly slower than the overall energy loop. This frequency decoupling will highly benefit differential current waveform: if not performed, overall energy and balance interaction leads to a really distorted differential current. This current, flowing in the phase-leg, would produce a voltage drop on the phase impedance, increasing losses and disturbances in the stability of the system.

VII. CONVERTER OPERATION MODEL

The first system implemented in MATLAB-Simulink includes only the equations in (3.2.11), but it is however important to understand the operation of the converter: in particular, the necessity of controlling the differential current and thus the energy stored in upper and lower arm becomes clear. In this simulation, output voltage and current are imposed and the operation of the system is then observed: modulation indexes are calculated ideally, neglecting differential voltage usage (no control strategy is implemented yet) and neglecting also the voltage drop of the output current on the arm parameters.

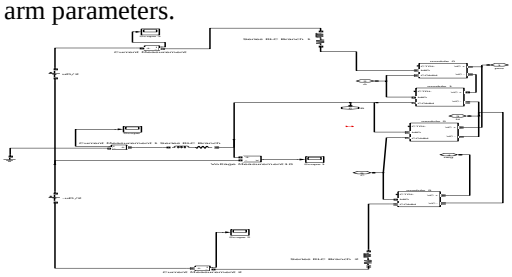

Fig 9. Model of MMC for HVDC system

Calculate the upper and lower arm current. Output voltage and current, and other system parameters are listed below in Table 1.

Table 1 List of system parameters

$u_V = 50\ \sin(\omega t)\ V$
$i_V = 10\sin(\omega t + \varphi)\ A$
$f = 50\ Hz$
$\varphi = 0$
$u_D = 200\ V$
$u_{CU}^{\Sigma}(ref) = 200\,V$
$u_{CL}^{\Sigma}(ref) = 200\,V$
$C^{arm} = 5\ mF$
$R = 0.1\,\Omega$
$L = 3\ mH$

VIII. CONTROL

Fig. 10 shows the schematic diagram of an MMC-HVDC system. When asymmetrical faults occur at the ac system, there will be negative- and zero-sequence components in grid voltages. In conventional converters with concentrated energy storage capacitors at the dc side (e.g., two-level converter), only positive and negative-sequence current components are fully controllable. Thus, the converter transformer is connected in the Y/Δ configuration to exclude the zero-sequence components from the converter. However, zero-sequence components will appear in the event of asymmetrical faults on the converter side of the converter transformer. On the other hand, zero-sequence components are unavoidable in transformer less scheme under asymmetrical fault conditions. In MMC, the distributed location of energy storage capacitors permits independent control of each phase. Thus, a zero sequence current control becomes possible in addition to the positive- and negative-sequence current control.

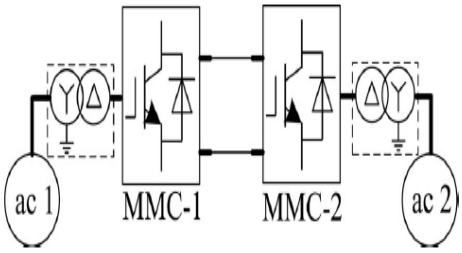

Fig. 10. Schematic diagram of an MMC-based HVDC system.

Control of Positive- and Negative-Sequence Currents If there are no zero-sequence components, only positive- and negative-sequence components are taken into consideration. The positive- and negative-sequence current control of conventional converters (e.g., two-level converter and three-level NPC converter), which is explained can be directly applied to MMC; therefore, a brief description is given here. The control scheme is divided into two separate loops: an inner fast current loop and an outer slow loop.

4.4.1 Inner Loop Current Control:

The inner current control is developed to regulate the positive- and negative-sequence currents at their command references by adjusting the control inputs respectively. The

ISSN: 2277-3754
ISO 9001:2008 Certified
International Journal of Engineering and Innovative Technology (IJEIT)
Volume 3, Issue 2, August 2013

disturbance inputs could be canceled by feed-forward compensation.

4.4.2 Outer Loop Control for Conventional Converters:
The outer loop control is designed to provide the command references for the inner loop current control. Two different power controllers have been proposed for conventional converters under unbalanced conditions [15]. The power controller 1 is developed to eliminate negative sequence Current components by setting their command references as zero [9], [15]. The power controller 2 is developed to eliminate the double line- frequency ripple in dc-side voltage by canceling the double line- frequency ripple in the three-phase real power input to the converter.

4.4.3 Outer Loop Power Controller for MMC:
In conventional converters (e.g., two-level converter and three-level NPC converter), the dc-side voltage is supported by centralized energy storage capacitors arranged at the dc side. The positive and negative-sequence components of the power ripple in each phase, which are circulating between three phases, have no effect on the three-phase real power and the dc-side voltage. In MMC, the energy storage capacitors are separately distributed in three phases and the dc-side voltage is supported by three phase units. Thus, power ripple in a single phase will result in a dc-side voltage ripple. Since power ripple in three-phase real power is eliminated with the power controller 2, the zero-sequence component in the single-phase power ripple is also eliminated. The dc-side voltage ripple at double line-frequency in conventional converters can be eliminated with the power controller 2. In MMC, not only the zero-sequence component but also the positive- and negative-sequence components of the power ripple in single-phase will cause dc-side voltage ripple. Thus, the dc-side voltage ripple in MMC cannot be eliminated with the power controller 2.

IX. SIMULINK MODEL AND RESULTS

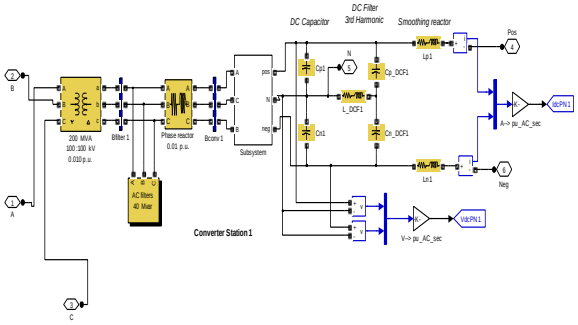

Fig 11. Simulink model of converter station 1 for HVDC system

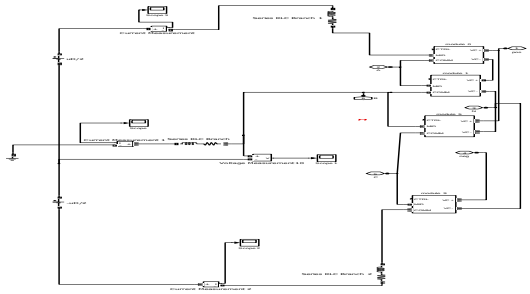

Fig 12. Simulink subsystem model of converter station 1 for HVDC system

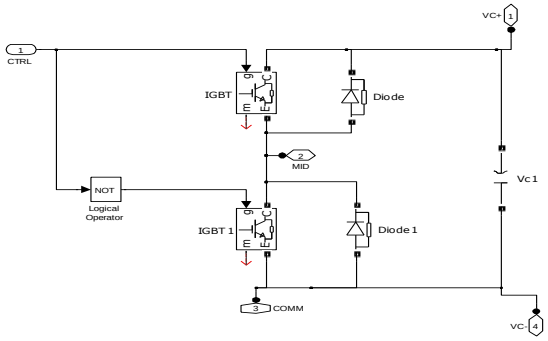

Fig 13 Simulink SM model of MMC for HVDC system

X. SIMULATION RESULTS

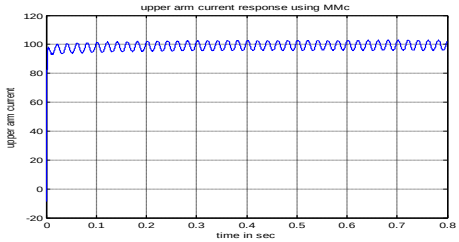

Fig 14.Simulation results of Upper arm current response using MMC

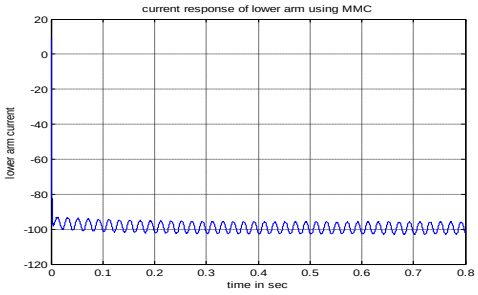

Fig 15 Simulation results of lower arm current response using MMC

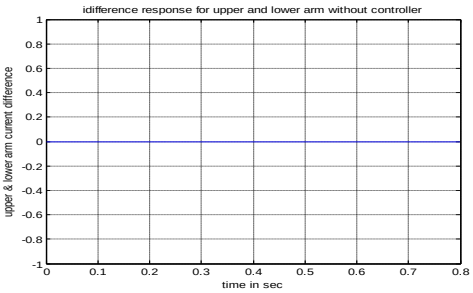

Fig 16 Simulation results of difference in current response for upper and lower arm without controller

ISSN: 2277-3754
ISO 9001:2008 Certified
International Journal of Engineering and Innovative Technology (IJEIT)
Volume 3, Issue 2, August 2013

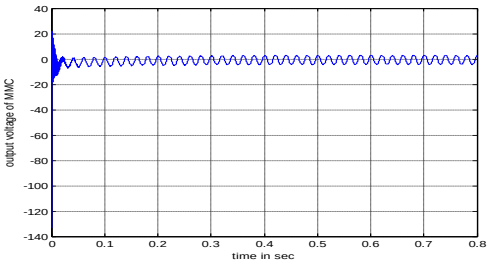

Fig 17 Simulation results of output voltage of MMC

XI. CONCLUSION

This paper presents a generalized mathematical model for MMC in realistic HVDC applications. In the model, as the number of levels in the converter increases, consequently, the number of redundant switching states increases. This thesis has provided a dc capacitor voltage balancing method for multi-level converters that in each sample of time selects the proper redundant switching states to solve the voltage drifting problem at the dc capacitors. From the simulation results, it is observed that the developed method is able to equalize the dc side capacitor voltages without using any additional power circuits. Based on the simulations, it is shown that among all the switching strategies, the provided balancing method leads to better capacitor voltage balancing at the side and also better harmonic spectrum for output voltage at the ac side. The aim of this project was the analysis of a Modular Multilevel Converter (MMC) for HVDC applications and the development of a control scheme to monitor the energy behavior. The analysis was based on the use of a simplified circuit, constituted by a single leg of the converter, where all the modules in each arm were represented by a single variable voltage source. The circuit model was derived as a system of differential equations, used for analyzing both the steady state and dynamic behavior of the MMC, from voltages and thus energy point of view.

REFERENCES

[1] N. Flourentzou, V. Agelidis, and G. Demetrius's, "VSC-based HVDC power transmission systems: An overview," IEEE Trans. Power Electron. vol. 24, no. 3, pp. 592–602, Mar. 2009.

[2] A. Lesnicar and R. Marquardt, "An innovative modular multilevel converter suitable for a wide power range," presented at the IEEE Power Tech Conf., Bologna, Italy, Jun. 2003.

[3] S. Allebrod, R. Hamerski, and R. Marquardt, "New transformer less, scalable modular multilevel converters for HVDC-transmission," in Proc. IEEE Power Electron. Spec. Conf., Jun. 2008, pp. 174–179.

[4] J. Dorn, H. Huang, and D. Retzmann, "A new multilevel voltage-sourced converter topology for HVDC applications," in Proc. Conf. Int. des Grands Reseaux Electriques, 2008, pp. 1–8

[5] M. Hagiwara and H. Akagi, "Control and experiment of pulse width modulated modular multilevel converter," IEEE Trans. Power Electron., vol. 24, no. 7, pp. 1737–1746, Jul. 2009.

[6] S. Rohner, S. Bernet, M. Hiller, and R. Sommer, "Modulation, losses and semiconductor requirements of modular multilevel converters," IEEE Trans. Ind. Electron., vol. 57, no. 8, pp. 2633–2642, Aug. 2010.

[7] M. Saeedifard and R. Iravani, "Dynamic performance of a modular multilevel back-to-back HVDC system," IEEE Trans. Power Del., vol. 25, no. 4, pp. 2903–2912, Oct. 2010.

[8] M. Hagiwara, R. Maeda, and H. Akagi, "Control and analysis of the modular multilevel cascade converter based on double-star chopper-cells (MMCC-DSCC)," IEEE Trans. Power Electron., vol. 26, no. 6, pp. 1649– 1658, Jun. 2011.

[9] L. Franquelo, J. Rodr´ıguez, J. Leon, S. Kouro, R. Portillo, and M. Prats, "The age of multilevel converters arrives," IEEE Ind. Electron. Mag., vol. 2, no. 2, pp. 28–39, Jun. 2008.[12] J. Rodr´ıguez, L. Franquelo, S. Kouro, J. Leon, R. Portillo, M. Prats, and M. Perez, "Multilevel converters: An enabling technology for high-power applications," Proc. IEEE, vol. 97, no. 11, pp. 1786–1817, Nov. 2009.

[10] M. Guan and Z. Xu, "Control and modulation strategies for modular multilevel converter based HVDC system," in Proc. 37th Annu. Conf. IEEE Ind. Electron. Soc., Nov., 2011, pp. 849–854.

[11] H. Song and K. Nam, "Dual current control scheme for PWM converter under unbalanced input voltage conditions," IEEE Trans. Ind. Electron. vol. 46, no. 5, pp. 953–959, Oct. 1999.

[12] A. Yazdani and R. Iravani, "A unified dynamic model and control for the voltage-sourced converter under unbalanced grid conditions," IEEE Trans. Power Del., vol. 21, no. 3, pp. 1620–1629, Jul. 2006.

[13] L. Xu, B. Andersen, and P. Cartwright, "VSC transmission operating Under unbalanced AC conditions–Analysis and control design," IEEE Trans. Power Del., vol. 20, no. 1, pp. 427–434, Jan. 2005.

[14] M. Saeedifard, R. Iravani, and J. Pou, "A space vector modulation strategy for a back-to-back five-level HVDC converter system," IEEE Trans. Ind.Electron., vol. 56, no. 2, pp. 452–466, Feb. 2009.

[15] K. Friderich, "Modern HVDC PLUS application of VSC in modular multilevel converter topology," in Proc. Int. Symp. Ind. Electron. Jul. 2010,.

AUTHOR'S PROFILE

Rinku scaria was born in Eranakulam, Kerala in 1989.She received B.Tech degree in Electrical and electronics engineering from Mahathma Gandhi University, Kerala and M.Tech from Anna University, Tamilnadu. EMAIL:rinkscaria89@gmail.com

Harikrishnan K was born in Trivandrum,kerala,in 1989.He received B.Tech degree in electrical and electronics engineering from kerala university and M.Tech in power electronics and power systems, from Mahathma Gandhi university, Kerala His research interests are in power electronic applications for the topology and control of active harmonic filter, power factor correction,HVDC systems EMAIL:harikrishnank6@gmail.com.