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A New Current-Mode Squarer Circuit For RMS-to-DC Converter

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Abstract*— In this paper a low-power current-mode RMS-to-DC converter is proposed. The converter includes two blocks: 1) squarer/divider circuit, 2) low-pass filter. These blocks employ CMOS transistors operating in weak inversion region. The proposed converter has low power consumption (<0.9µW), low supply voltage (0.9V), wide input range (from 1 nA to 400 nA), low relative error (<4 %), and low circuit complexity. Comparing the proposed circuit with two other current-mode circuits shows that the proposed circuit operates better than two other converters in terms of power dissipation, supply voltage, and complexity. Simulation results by HSPICE show high performance of the circuit and confirm the validity of the proposed design technique.

***Keywords*- current-mode; squarer/divider; RMS-to-DC converter; weak inversion; low power; low voltage.**

I. INTRODUCTION

The RMS-to-DC converter as an electronic measuring circuit is employed for computing of the average energy content in an electronic signal. This converter is widely used in instrumentation devices and biomedical Ics.

Recently, researchers focus on small size, low power consumption and capable to operate under low supply voltage while the performance still maintains. Most of RMS-to-DC converters with CMOS transistor in saturation region have power consumption of about 100uW and required the supply voltage of about 1.5V [1-2], which is not suitable for very low power applications such as in biomedical Ics [3]. In addition, a micro power CMOS true RMS-to-DC converter has been proposed [4], however they design based on CMOS transistor operating in saturation region combination with FG-MOS operating in weak inversion region which is complicated synthesis for the integrated circuit. The two approaches exist for designing RMS-to-DC converter: 1) current-mode approach, 2) voltage-mode approach. A current-mode circuit enables current processing and has certain important advantages against a voltage-mode circuit, such as, wide bandwidth, high slew rate, low power consumption, and simple circuitry [5-6].

The proposed circuit of RMS-to-DC converter in this paper includes four current-mode blocks; (a) squarer (b) low-pass filter. All of them designed based on the use of CMOS transistors operating in weak inversion region. The main features of this circuit is its low-power (<0.9µW), requires low supply voltage of 0.85V for the input range of 1nA to 400nA and simplicity of the circuit design. The other feature of this circuit is that the converter doesn't have additional power source, then it causes lower power compared to other converter.

The paper is organized as follows. In section II the basic principle of converter is described. Circuit design of the proposed converter is explained in section III and the circuit analysis of the proposed converter is presented. The characteristics and the performances of the converter are presented by HSPICE simulation results in section IV and conclusion is provided in section V.

II. BASIC PRINCIPLE

One of the most notable instances of nonlinear dynamic operation from a practical viewpoint is the RMS-to-DC conversion. In its basic form, and assuming input and output currents, such operation can be described by the equation:

$$I_{out} = \sqrt{\langle I_{in}^2 \rangle} \tag{1}$$

Where I_{in} and I_{out} are the input and output currents of the RMS-to-DC converter, respectively, and the operator $\langle ... \rangle$ Represents a time averaging. A (mathematically equivalent) approach, better in terms of offset [7], is given by

$$I_{out} = \left\langle \frac{I_{in}^2}{I_{out}} \right\rangle \tag{2}$$

Hence, two operations have to be performed: squaring/division and subsequently, averaging. Fig. 1 shows the block diagram of the current-mode true RMS-to-DC converter which consists these two operations.

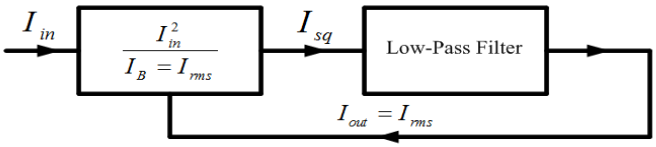

Fig 1. Block diagram of RMS-to-DC converter

III. CIRCUIT ANALYSIS OF THE PROPOSED CONVERTER

The ratio of V/I for MOSFETs transistors operating in weak inversion region can be obtained from equation (3) [8]:

$$V_{GS} = \xi\, V_T \ln\left(\frac{I}{(W/L).I_{0n,p}}\right) \tag{3}$$

Where $I_0 = I_S e^{\wedge}(V_{th-n,p} / \xi V_T)$, $V_T = kT/q$ $I_S = 2\xi\, \mu_{n,p}\, C_{ox} (V_T \wedge 2)$, and $\xi > 1$. Except for ξ, equation (3) is similar to the exponential I_C / V_{BE} relationship in a bipolar transistor. Principle of operation for squarer circuit is based on translinear loops. The proposed squarer which uses four NMOS transistors is shown in Fig. 2.

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I_{in} the input current which enters into sources of M2 and drain of M1 . Considering Fig. 2, M1-M2 and M4-M5 form a translinear loop. The relationship between these four transistors can be described as [3]:

$$\sum_{CW} V_{GS} = \sum_{CCW} V_{GS} \tag{4}$$

$$\xi V_T \ln\left(\frac{I_1}{\left(\frac{W}{L}\right)_1 I_0}\right) + \xi V_T \ln\left(\frac{I_2}{\left(\frac{W}{L}\right)_2 I_0}\right) =$$

$$\xi V_T \ln\left(\frac{I_4}{\left(\frac{W}{L}\right)_4 I_0}\right) + \xi V_T \ln\left(\frac{I_5}{\left(\frac{W}{L}\right)_5 I_0}\right) \tag{5}$$

Considering Fig. 2, $(W/L)_1 = (W/L)_2$ and $(W/L)_4 = (W/L)_5 = 2(W/L)_1$, also currents of M1-M2 and M4-M5 are equals to:

$$I_1 = (I_{out} + I_{in})/2 \tag{6}$$

$$I_2 = (I_{out} - I_{in})/2 \tag{7}$$

$$I_4 = I_{out} - I_B \tag{8}$$

$$I_5 = I_{out} \tag{9}$$

According to equation (5) to (9), output current of squarer is equal to:

$$I_{sq} = I_{out} = I_{in}^2 / I_B \tag{10}$$

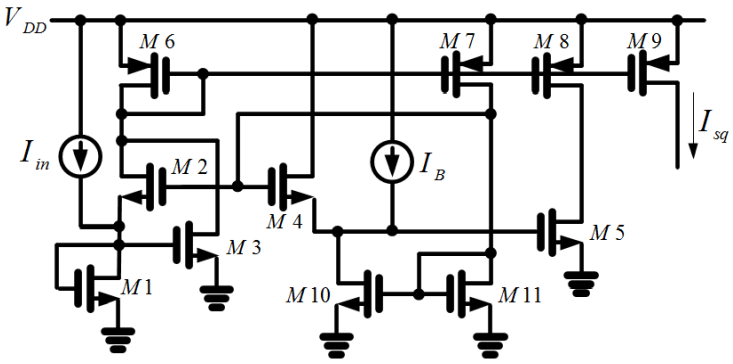

Fig 2. The proposed current-mode square circuit which is used in RMS-to-DC converter

For a current-mode first order low-pass filter, output current I_{out} and input current I_{sq} in laplace domain are related as :

$$\frac{I_{out(s)}}{I_{sq(s)}} = \frac{1}{1+\frac{s}{\omega_c}} \rightarrow I_{out(s)} + \frac{s}{\omega_c} I_{out(s)} = I_{sq(s)} \tag{11}$$

Time domain of equation (11) is equal to :

$$\frac{1}{\omega_c}\frac{dI_{out(t)}}{dt} = I_{sq(t)} - I_{out(t)} \tag{12}$$

In which, $\omega_c = 1/\tau$ is the cutoff frequency of filter. Fig. 3 shows the circuit of the proposed low-pass filter.

For the I-V relationships of transistor Mf1 in weak inversion region and its derivation can be expressed by:

$$I_{out} = (W/L) I_0 e^{\frac{V_C}{\xi V_T}} \rightarrow \frac{dI_{out}}{dt} = \frac{1}{\xi V_T}(W/L) I_0 e^{\frac{V_C}{\xi V_T}} \frac{dV_C}{dt}$$

$$\rightarrow \frac{dI_{out}}{dt} = \frac{I_{out}}{\xi V_T}\frac{dV_C}{dt} \tag{13}$$

In which, V_{gs} is the voltage of capacitor C ($V_{gs} = V_C$). Using (13) and also $I_C = C(dV_C/dt)$, it results :

$$\frac{dI_{out}}{dt} = \frac{I_{out}}{\xi V_T}\frac{I_C}{C} \tag{14}$$

And then, substituting (14) into (12) gives :

$$\frac{1}{\omega_c}\frac{I_{out}}{\xi V_T}\frac{I_C}{C} = I_{sq(t)} - I_{out(t)} \tag{15}$$

Considering $I_{C(t)} = I_{sq(t)} - I_{out(t)}$ and equation (15), $(1/C\omega_c)(I_{out}/\xi V_T) = 1$. Therefore, cutoff frequency of the filter is equal to :

$$\omega_C = I_{out}/\xi V_T C \tag{16}$$

It can be shown that, for the input signal whose frequency is more than five times the cutoff frequency of the filter, output ripple will be less than 1% [9]. In such case, the output current of the RMS-to-DC converter is a DC current (I_{rms}) with an ac ripple on it. The amplitude of this ripple is small compared to I_{rms}, i.e., $I_{out1} \cong I_{rms}$. Considering these conditions and also using (16) it results that the values of the capacitor to ac9hieve the accuracy of more than 1% is :

$$C \geq \frac{5I_{rms,MAX}}{\xi V_T (2\pi f_{\min})} \tag{17}$$

Where $f_{\min}$ is the lowest frequency of the interested frequency range.

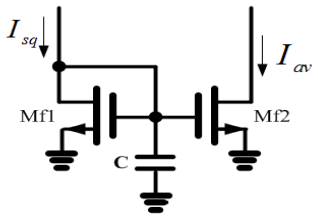

Fig 3. The proposed first-order

For example, if the amplitude of the sinusoidal input current $I_M = 400nA$, $f_{\min} = 100Hz$ and ripple error of 1%, then the averaging capacitance of $C = 15nF$ must be chosen. Considering equation (17), it's obvious if frequency

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increases then the capacitance of C decreases. Therefore, the ripple error diminishes by increasing of frequency. Completed circuit of the proposed RMS-to-DC converter is shown in Fig.4.

IV. Simulation Results

The performance of the circuit has been evaluated using simulation with HSPICE by level 49 parameters (BSIM3v3.2) in 0.18µm standard CMOS technology. $V_{DD} = 0.9$ V and $C = 15$ nF were employed. The aspect ratio of the transistors is shown in Table I. I_{rms} is shown in Fig. 5 for the sinusoidal input signal with peak amplitude of 400nA and 1nA at frequency of 100Hz, respectively. The relative error, calculated by equation (18), is depicted in Fig.6 for different amplitudes of the sinusoidal input currents and for CMOS process corners. A less than 4% error is achieved for amplitudes between 1nA and 400nA.

$$\text{Relative error} = \frac{I_{rms}(theoretical) - I_{rms}(simulated)}{I_{rms}(theoretical)} \times 100\% \quad (18)$$

	M1-M3,M10-M13	M4-M5	M6-M9,M14-M15
L(µm)	0.5	0.5	1.2
W(µm)	1	2	1.2

TABLE I. Simulation Results

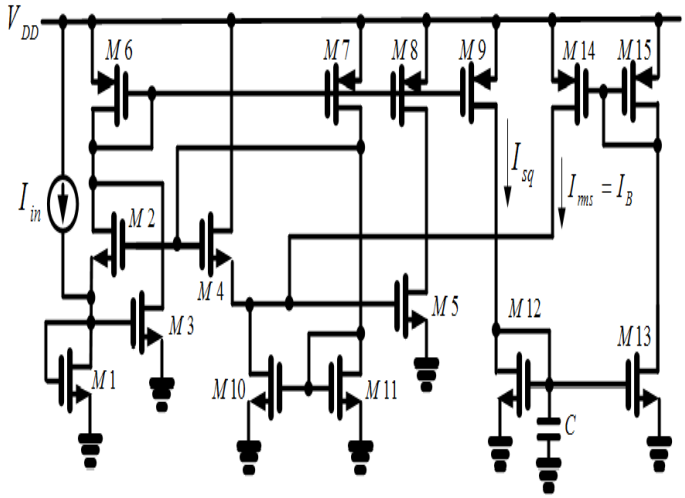

Fig 4. Complete circuit diagram of the proposed RMS-to-DC converter

Simulation results show that the power consumption of the circuit for the maximum accepted input current (400nA) is less than 900nW. The comparison results, shown in Table.2. indicate that the proposed converter has better performance than two other current-mode converters in terms of power dissipation, supply voltage, and complexity. The proposed converter is compared with other current-mode circuits is [5-6]. The comparison results, shown in Table. 2., indicate that the proposed converter outperforms the two other current-mode converters in terms of power dissipation, supply voltage, and complexity.

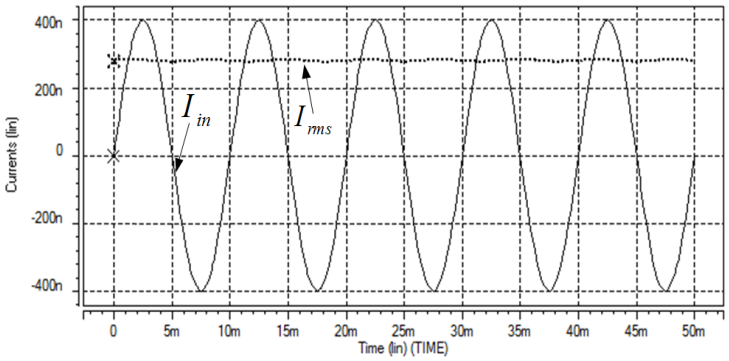

Fig. 5. Time response of output current of the RMS-to-DC converter for a sinusoidal input with peak amplitude of 400nA at frequency of 100Hz.

V. Conclusion

In this paper, a very low-power, low-voltage two-quadrant current-mode RMS-to-DC converter based on MOS translinear principles operating in weak inversion region is presented. Simulation results have been given to confirm the validity of the theoretical analysis. According to results, the converter has low power consumption (900nW), low power supply voltage (0.9V), and wide input range (1nA to 400nA). Relative error of this converter for corner cases indicates that the proposed circuit is not dependent on variation of fabrication.

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AUTHOR'S PROFILE

Mohammad Hadi Danesh was born in Marvdasht, Iran, in 1989. He is currently pursuing his M.Sc. degree in Iran University of Science and Technology, Electrical and Electronic Engineering School. He is with Electronic Research Center Group, since 2011 and cooperates with Islamic Azad University-Eyvankey Branch (sama) and Eyvankey Institute of Higher Education. His current research interests include current mode integrated circuit design, low voltage, low power circuit and systems, analog microelectronics, and RF design.

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APPENDIX

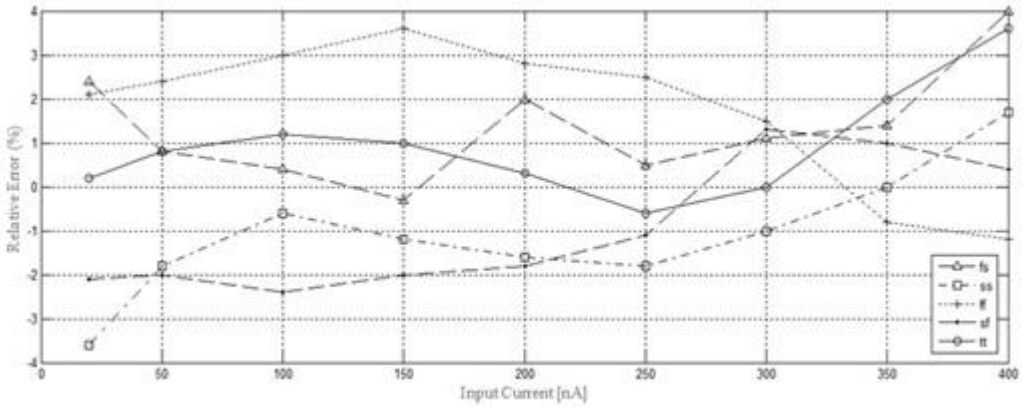

Fig. 6. Relative error vs. input current amplitude of the RMS-to-DC converter

TABLE II. A COMPARISON BETWEEN RMS-TO-DC CONVERTERS.

Parameter	Ref.[5]	Ref.[6]	Proposed circuit
Basic principle	Log-domain MOS	class-AB transconductance	Log-domain MOS
Technology	0.18µ	0.5 µ	0.18 µ
Supply voltage	1 V	1.5 V	0.9 V
Power dissipation	<3 µW	>100 µW	<0.9 µW
Circuit complexity (transistor no.)	42 MOS	40 MOS	15 MOS
Input range	50nA-500nA@3%R.L	12µA-22µA@3%R.L	1nA-400nA@4%R.L