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Design of Low-Voltage Operational Amplifier (700mV)

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Abstract: ***Now-a-days there are many digital and analog circuits that are implemented by CMOS VLSI technology. Currently CMOS VLSI is progressing at fast rate and dominating most of the market. The low voltage VLSI circuits represent the electronic of the future. All electronics products are striving to reduce power consumption, to create more economical and efficient devices. For deep sub-micron CMOS technology the technique required to operate the circuit at low voltage is challenging. As power is directly related to the voltage in order to make a low power CMOS VLSI circuits we need to find an appropriate low voltage CMOS VLSI circuit. Here in this paper we have demonstrated a small signal low voltage operational amplifier operating at 700mV power supply.***

Keywords: **Low Voltage OP-AMP; Small Signal OP-AMP; Low Power Circuits; Low Voltage Circuits; Design of OP AMP.**

I. INTRODUCATION

CMOS technology is most suitable for realizing VLSI system because of continuous downscaling of the CMOS which results in the increased driving current, reduced parasitic, reduced power dissipation per gate, increased packing density and reduced cost. When the channel length is scaled down, the lateral electric field in a device increases to a large extent, degrading the device reliability and due to decrease in gate oxide thickness vertical electric field also increases resulting in decrease oxide [1]. In order to reduce these field, (vertical and lateral), reduction of power supply voltage is the necessary prerequisite. Increased power consumption results in raised ambient temperature degrading the device performance [2].Thus a VLSI chip requires a good packaging for dissipating heat. For present day high performance VLSI design cooling device such as fan may be required. Efficient power dissipation of CMOS VLSI chip is a challenge for the engineering CMOS VLSI system with continuously down scaling of the CMOS device Thus lowering of the power supply voltage is the most efficient method in reducing power dissipation of the CMOS VLSI chip. Now-a-days with the advancement in the technology emphasis is being laid on longer battery life which can be easily accomplished by reducing the power requirement of the circuit as the advancement in the CMOS VLSI is much more in comparison to the advancement in the battery technology [3]. Here we have designed a low voltage operational amplifier with the priority of reducing the voltage supply of the circuit rather than any other parameter of the circuit.

II. METHODS

The low voltage operational amplifier is built in the Redhat UNIX environment and the tool used is Cadence Virtuoso. The technology used in this case is 180nm. Most of the analysis ranging from various operational amplifier parameters, like CMRR, PSRR etc., to low power analysis is done on the 180nm technology. However in order to show the significance of the decrease in the size of the gate we have used 90nm technology to measure the cut off frequency of the same circuit. The cut off frequency at different voltage supply is shown on 180nm technology. All the analysis of the operational amplifier is done on 2.3 V power supply.

III. THEORY

Here in this project we have designed a two stage OP-AMP. The OP-AMP in this project includes four major circuitries – a biasing circuit, an input differential amplifier, a second gain stage and a compensation network. Inputs of differential amplifier behave as the inputs of the operational amplifier and provide a good portion of the overall gain to improve noise. The second gain stage is typically configured common source stage so as to allow the maximum output swings. The bias circuit is provided to establish the proper operating point for each transistor in its saturation region. Here the biasing circuit is implemented using the current mirrors.

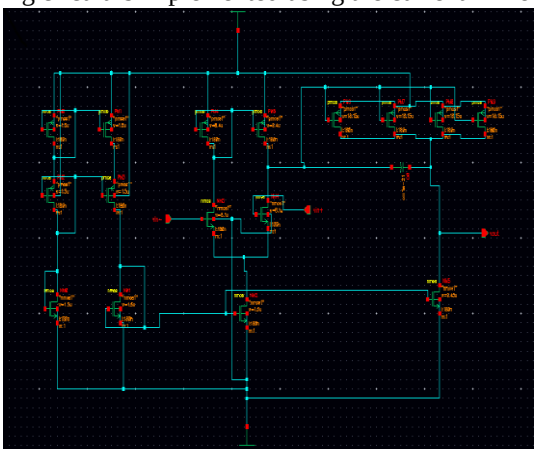

Fig. 1. Schematic of small signal low voltage OP-AMP

The advantage of using current mirrors is that the each current mirror can be considered as a individual current source. The forth part of the circuit the compensation network is used to maintain the stability when the negative feedback is applied to the operational amplifier [4]. The cut off frequency was calculated at different

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power supply voltage ranging from 700mV to 3.3V. However various parameters of the OP-AMP was calculated at the 2.3V power supply. The schematic shown in figure 1 is converted into appropriate block representing an OP-AMP, which is then used for different analysis and low power analysis.

IV. RESULTS

The result of the different analysis in 180nm technology is listed below in tabular form. The cut off frequency at different voltage is shown in table 1. Different parameters of the OP-AMP as shown in table 2 were calculated at 180nm technology keeping the voltage source constant 2.3V for all the analysis.

Table 1: Cut off frequency at different voltages

Supply Voltage	Cut off Frequency
700Mv	100KHz
1V	1MHz
1.3V	5MHz
1.8V	10MHz
2.3V	20MHz
3.3V	100MHz

Table 2: OP-AMP Specifications

Specifications	Value
Gain	51dB
ICMR	-2.3V to 2.3V
CMRR	64dB
PSRR-	50dB
PSRR+	45dB
O/P Voltage Swing	-2.3V to 2.2V

V. DISCUSSION

When the same schematic was implemented in 90nm technology on cadence virtuoso at 2.3V power supply the cut off frequency reached up to 1GHz which was 20MHz at the same power supply in 180nm technology. So it can be seen that with the advancement in the sub-micron technology, high cut off frequency is witnessed.

VI. CONCLUSION

Looking at the result we can conclude that we were successful in creating low voltage OP-AMP. However the use of a particular type of OP-AMP depends upon the requirement of the circuit. But in the circuitry where low power is the foremost requirement, such as in mobile devices, this OP-AMP can be extremely useful.

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REFERENCES

[1] B. Davari, R. H. Dennard, and G. G. Shahidi. (1995). CMOS Scaling for High Performance and Low Power-The Next Ten Years, IEEE Proc., 83(4), 595–606.

[2] T. Kuroda and T. Sakurai. (1995). Overview of Low-Power ULSI Circuit Techniques. IEICE Trans. Electron., E78-C (4), 334–343.

[3] James B. Kuo, Jea-Hong Lou. (1999). Low-Voltage CMOS VLSI Circuits. John Wiley & Sons.

[4] Phillip E. Allen, Douglas R. Holberg. (2002). CMOS Analog Circuit Design Second Edition. Oxford University Press.