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Design Optimal Controller For Reduce Voltage Flicker and Harmonic Distortion in Power System Base on SVC

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Abstract*— The present paper aims at utilizing the Static VAR Compensator SVC for simultaneously load balancing and voltage flicker elimination due to arc furnace loads. The SVC of thyristor controlled reactor-fixed capacitor TCR-FC type is considered. Due to the latest achievements in the semiconductors industry and consequently the emergence of the compensators based on voltage source converters, FACTS devices have been gradually noticed to be used for voltage flicker compensation. The reason for this disturbance is mainly the large nonlinear loads such as electric arc furnaces. In this paper, SVC has been proposed for effective mitigation of Voltage flicker and reduction of total harmonic distortion in the system. In simulation we estimate controller parameter with NSGA II algorithm and calculate total harmonic distortion (THD) of signals in case study system. The obtained results show that SVC is very efficient and effective for the flicker compensation as well as harmonic spectrum. All the simulations have been performed using MATLAB Software.

***Index Terms*— Voltage flicker, SVC, Nonlinear load, NSGA-II, Harmonic Distortion.**

I. INTRODUCTION

In recent years, power quality in power systems becomes very important due to the growth of the industrial plants, increase in the energy consumption and diversity of the electrical loads [1]. Voltage flicker is one of the common problems that have a negative effect on the power quality. Electric arc furnace (EAF) is an important load in industry with very large active and reactive time varying powers in the melting and refining processes period which causes irregular voltage oscillation at the point of common coupling (PCC) [2]. This leads to an undesirable effect on the electric light sources, power electronics devices (within protective relays) and their lifetime [3]. IEEE519-1992 indicates that only 0.5% changes in the voltage amplitude leads to light intensity change which harms the human eyes [4, 5]. So voltage flicker mitigation is essential for the power systems. Various techniques for reduction of the buses voltage fluctuations, below the standard limit, have been so far introduced. Considering the nature of the voltage flicker, which is rapid and unpredictable, a compensator used must quickly response to the voltage fluctuations and variations. Other important factors including non-bulky compensator (drawback of SVC), suitable harmonic behavior, unlimited kVar (drawback of active filters), disuse of expensive tools (drawback of smart trafo) [6], DG algorithm [3, 7], UPFC [8] and unlimited line commutation (drawback of dynamic phase controlling method) [9], must be taken into account. Among various compensators that have been so far introduced, STATCOM has the above-mentioned features and is a desirable technique for voltage flicker mitigation [10]. Primary duty of the STATCOM is regulating the voltage in order to improve the voltage profile of the power system [11].The factor that plays a very important role in the improvement of the STATCOM performance is the use of power electronics converter as the core of the STATCOM. A more precise performance of the converter leads to a more precise compensator. In this paper, a three-level 12-pulsed PWM voltage source inverter (VSI) with a 12-terminal transformer connected to the ac system is proposed. It is expected that this structure is more precise than that of the simple two-level type, because a 12-pulsed three-level converter offers better sinusoidal waveform compared to that of the two-level one. On the other hand, a lower voltage harmonic leads to the use of low-voltage switches which are quicker, smaller and cheaper than that of the high-voltage switches in two-level case. In addition, a lower the THD, lower switching losses due to the lower switching frequency, a better overall efficiency of the system at full-load and consequently a smaller heat-sink and higher reliability are the other advantages of the three-level converters compared to that of the two-level converters [12]. As reported in [12], the total losses of the two-level converter are 44% higher than that of the three-level one. However, the two-level converter is 27% cheaper than that of the three-level configuration. The reasons are the dc link capacitors, IGBTs and more diodes and more complicated control strategy in the three-level converter. It is noted that the output dv/dt in the three-level converter is smaller than that of the two-level converter and consequently it has less stress on the cables [13]. To eliminate the voltage flickers caused by arc furnace loads, several methods have been applied such as connecting synchronous condenser with buffer reactor. The present paper investigates an application of static VAR. compensator for simultaneous elimination of voltage flickers and three-phase current imbalance due to arc furnace loads.

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II. MODEL OF AN ELECTRIC ARC FURNACE CIRCUIT

Fig. 1 shows a single phase simplified network of an electric arc furnace EAF load comprising of supply network, furnace transformer connections, and location of compensator connection. The supply network, furnace transformer and cable resistances (excluding the resistance of the arc itself) are of much lower magnitude than their reactance values [12–15]. While Fig. 2 depicts the computer simulated single phase EAF model in which the arc characteristic is represented as a randomly varying resistance (ρ)

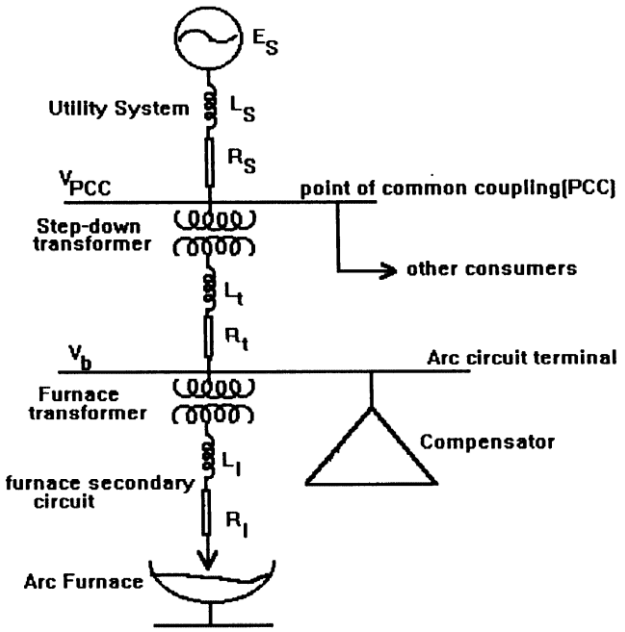

Fig. 1. Single phase supply network diagram of an electric arc Furnace

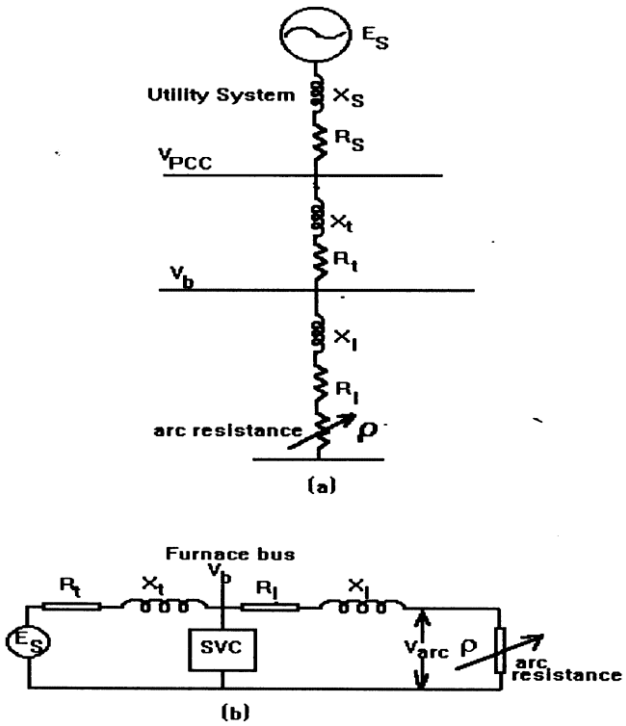

Fig. 2. Derivation of single-phase equivalent circuit for estimating furnace operating characteristics

The three basic changes in operating states of an EAF which can produce distinguishable voltage disturbances on a power system are shown in Fig. 3. In extreme conditions, the furnace load may change from complete open circuit to a full three-phase short circuit condition several times during a furnace heat. During normal operation irregular voltage fluctuations or voltage flicker will occur as a consequence of arc movement. Low level frequency modulation of the supply voltage of less than 0.5% can cause annoying flicker in lamps and invoke public complaints when the frequency lies in the range of 6–10 Hz [15]. There is a need therefore to develop better techniques to compensate the voltage flicker [16– 23]. It is found that the three-phase resistances and reactance's of the furnace transformer connection are not symmetrical. Further, the three-phase arc circuit impedances and arc resistances are not equal. Therefore, the three-phase line currents are unbalanced.

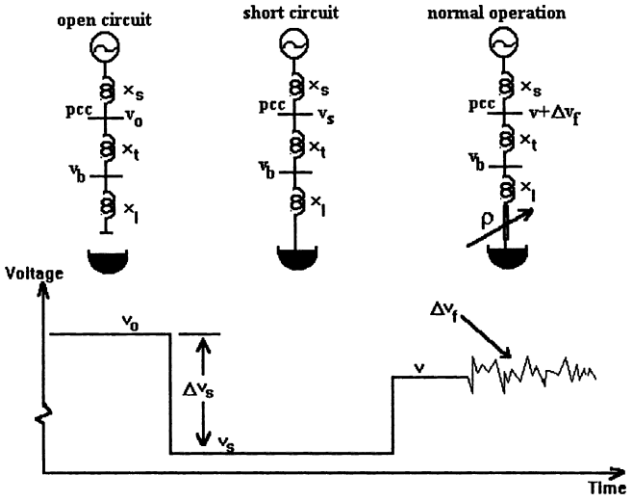

Fig. 3. Voltage changes due to operating state of an electric arc furnace

SVC CONTROLLER DESIGN

A typical block diagram of a SVC controller is shown in Fig. 4. The difference of the actual voltage at the point of common coupling Vpcc and the reference value is given as input to the PI control block. The PI controller consists of gain constant, Kp, and integral constant Ti. These are the parameters that need to be optimally selected for the SVC to ensure optimal system performance under a wide range of operating conditions and disturbances. *B*, susceptance value of the SVC is the output of the PI control block. *B*max and *B*min are the limits for *B*.

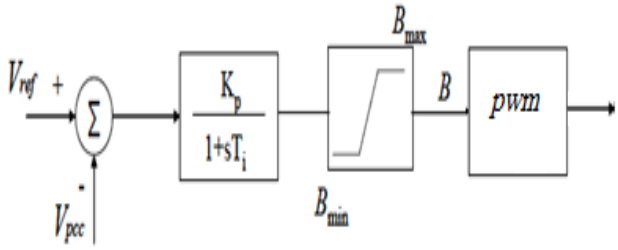

Fig.4. Block diagram of SVC PI controller.

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III. NSGA-II ALGORITHM

The basic idea behind NSGA is the ranking process executed before the selection operation [14-20]. The ranking procedure consists to find the no dominated solutions in the current population *P*. These solutions represent the first front *F1*. Afterwards, this first front is eliminated from the population and the rest is processed in the same way to identify no dominated solutions for the second front *F2*.showing in figure 5.

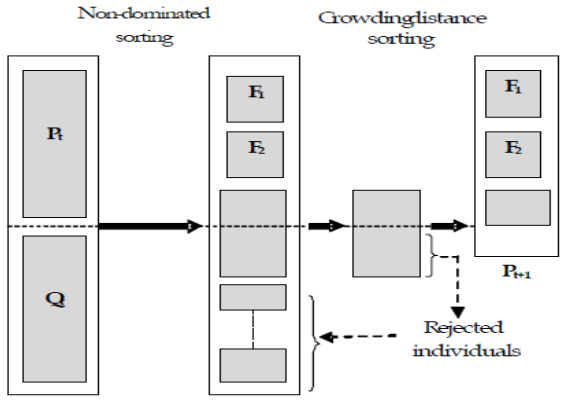

Fig. 5. NSGA-II procedure

In this approach, the sharing function approach is replaced with a crowded comparaison.Initially, an offspring population *Qt* is created from the parent population *Pt* at the *tth* generation. After, a combined population *Rt* is formed :

$$Rt = Pt \cup Qt \quad (5)$$

Rt is sorted into different no domination levels *Fj* as shown in the NSGA approach. So, we can write :

$$R_t = \bigcup_{j=1}^{r} F_{j_t} \quad (6)$$

Where, *r* is number fronts. Finally, one iteration of the NSGAII procedure is as follows:

Step 1 : Create the offspring population *Qt* from the current population *Pt* .

Step 2 : Combine the two population *Qt* and *Pt* to form *Rt* .

Step 3 : Find the all nondominated fronts *Fi* and *Rt* .

Step 4 : Initiate the new population *Pt*+1 = *Ó* and the counter of front for inclusion *i* = 1.

Step 5:While $|P_{t+1}| + |F_i| \le N_{pop}$ do:

$$Pt+1 \leftarrow Pt+1 \cup Fi \quad i \leftarrow i+1 \quad (7)$$

Step 6 : Sort the last front *Fi* using the crowding distance in descending order and choose the first

(*Npop* − *Pt*+1) elements of *Fi* .

Step 7 : Use selection, crossover and mutation operators to create the new offspring population *Qt*+1 of size *Nobj* . To estimate the density of solution surrounding a particular solution *X i* in a nondominated set *F*, we calculate the crowding distance as follows:

Step 1 : Let's suppose *q* = | *F*| . For each solution *X i* in *F*,set *di* = 0 . Initiate *m* =1

Step 2 : Sort *F* in the descending order according to the objective function of rank *m*.

Let's consider $I^m = sort_{[f_m>]}(F)$ the vector of indices, i.e. I_i^m is the index of the solution *X i* in the sorted list according to the objective function of rank *m*.

Step 3 . For each solution *X i* which verifies

$$2 \le I_i^m \le (q-1) \quad (8)$$

update the value of *di* as follows:

$$d_i \leftarrow d_i + \frac{f_m^{I_i^{m+1}} - f_m^{I_i^{m-1}}}{f_m^{max} - f_m^{min}} \quad (9)$$

Then, the boundary solutions in the sorted list (solutions with smallest and largest function) are assigned an infinite distance value, i.e. if, *m* 1 *i I* = or *im I* = *q* , *di* = ∞ .

Step 4 : If *m* = *M* , the procedure is finished. Else, *m* = (*m*+1) , and return to step 2.

The proposed method flowchart showing in figure 6.

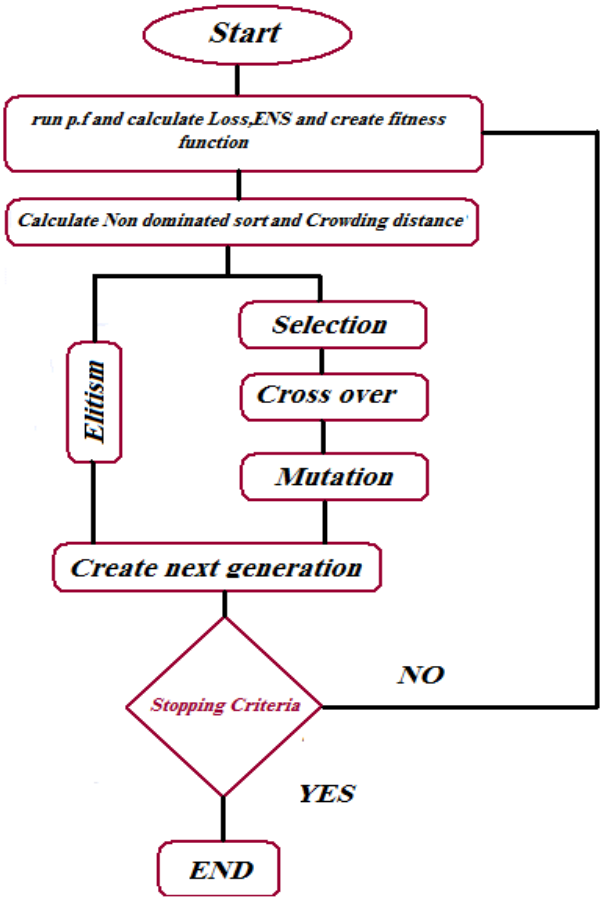

Fig.6. The proposed NSGA II Algorithm

IV. SIMULATION AND RESULT

Figure 7 showing the test system that A ***Static VAR Compensator*** (svc) is used to regulate voltage on a 25-kV distribution network. The feeder (21 km) transmit power to

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loads connected at buses B1 and B2. The 600-V load connected to bus B2 through a 25kV/600V transformer represents a plant absorbing continuously changing currents, similar to an arc furnace, thus producing voltage flicker. The variable load current magnitude is modulated at a frequency of 5 Hz so that its apparent power varies approximately between 1 MVA and 5.2 MVA, while keeping a 0.9 lagging power factor. This load variation will allow you to observe the ability of the SVC to mitigate voltage flicker. The SVC regulates bus B2 voltage by absorbing or generating reactive power. This reactive power transfer is done through the leakage reactance of the coupling transformer by generating a secondary voltage in phase with the primary voltage (network side). This voltage is provided by a voltage-sourced PWM inverter. When the secondary voltage is lower than the bus voltage, the SVC acts like an inductance absorbing reactive power. When the secondary voltage is higher than the bus voltage, the SVC acts like a capacitor generating reactive power.

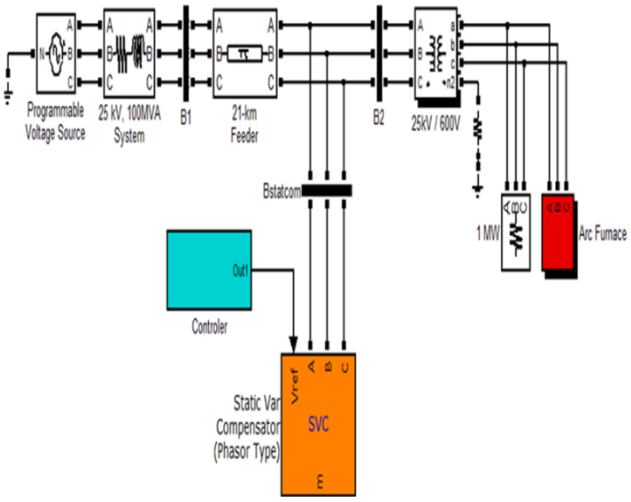

Fig.7. simulink model of under study system

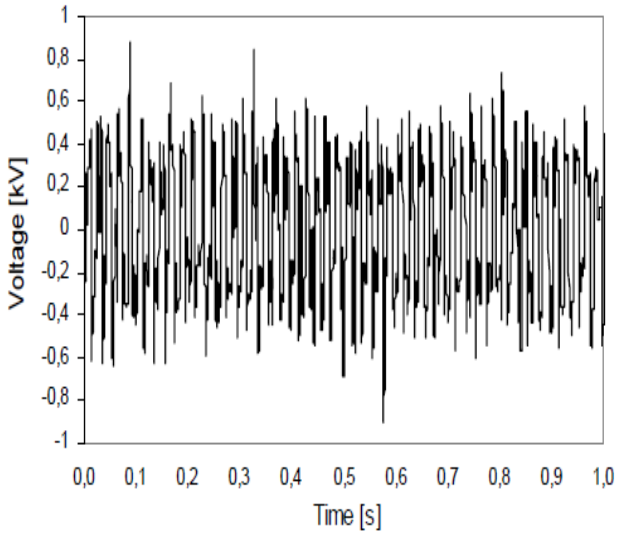

Fig.8. Voltage waveform at the Arc Furnace

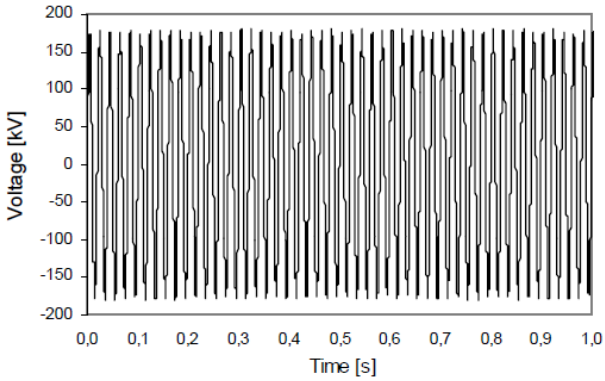

Fig.9. Voltage waveform at the PCC (Bus 2)

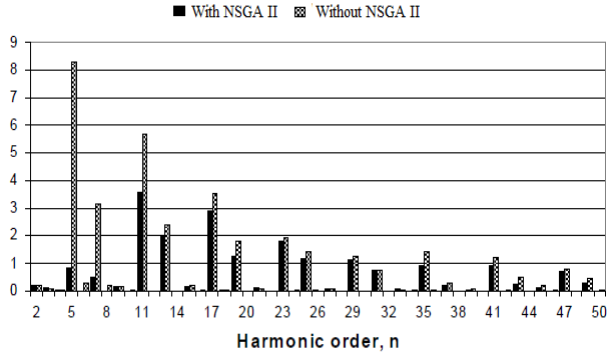

Fig .10. Voltage distortion on nonlinear load when breaker closed

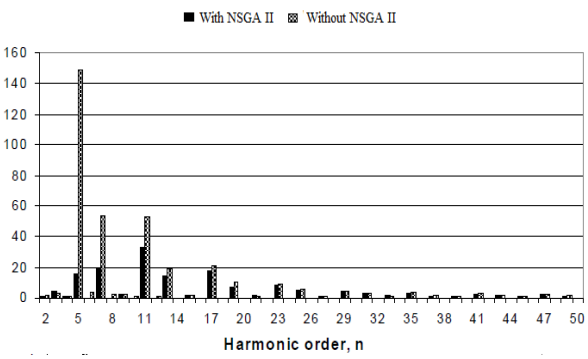

Fig .11. Current distortion on nonlinear load when breaker closed

V. CONCLUSION

The cross coupling between the fundamental voltage and current harmonics is strong close the non-linear loads. The non-linearity is more or less obvious depending of the configuration of the network and the composition of loads, linear and non-linear. The NSGA II algorithm has been implemented in a commercial power system simulation tool with detailed nonlinear models of the power system elements. The potential of the NSGA II algorithm is valuable for large power systems with multiple SVCs and other controllers where optimization of controller parameters is necessary to avoid any adverse effects. Background voltage distortion, caused by single phase non-linear loads, reduces the current distortion from these loads. In addition, the NSGA II algorithm is feasible for reduce *harmonic* distortion in power system. A short overview is given of the most important

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subjects that are to be studied to access the consequences of harmonic distortion and for the modeling of the system with loads.

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