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Establishment of connection between parameters of CMOS inverter for Static force Optimization

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Abstract*— This paper presents a portrayal of the prevailing qualities of the CMOS inverter, which is utilized for voltage converters–charge siphons applications. This circuit controls transport charge between primary capacitors to make a higher DC voltage. The critical aspect of the siphon misfortunes is brought about by the inverter cross current. This current courses through the inverter on the move state and releases the capacitor, accordingly diminishes the siphon voltage gain. The CMOS inverter configuration depends on the simple square depiction for high-voltage coordinated circuits utilizing BSIM model conditions. The main advantage of this paper is to derivate and investigative connection between width and length of the NMOS and PMOS semiconductors to accomplish the static force minimization. The determination has been performed dependent on the affectability examination. The quality of the proposed circuit has been confirmed by reenactment in ELDO Spice. Examination results show that the cross current is diminished by multiple times in correlation with the estimation of the standard advanced inverter (with balanced voltage move qualities). This improvement was accomplished while keeping moderately enormous region of the two semiconductors fulfilling the dynamic properties.

***Index Terms*—CMOS inverter, BSIM model, high-voltage, sensitivity.**

I. INTRODUCTION

A CMOS inverter is a basic block (Fig. 1) for digitaldesign circuits which performs a logic operation from A to A.However, there are also aplications in the analog domain; bothcontinuous–time circuits (oscillators, amplifiers) and discrete–time analog circuits (voltage convertors). Although discrete–timeanalog circuits seem to be digital circuits from a system perspective, the internal state of the system is time continuousduring each period of the clock signal. Results of the transientanalysis show that the dominant part of losses in chargepumps is caused by a DC cross current that flows throughan inverter operating in the linear region of voltage transfercharacteristics. This is undesirable *because the cross current greatly decreases a pump´s voltage gain* while losses causedby propagation delays of the inverter are very small.

Current research deals with the dynamic behavior of theinvertor and transistor sizing, which is based on the *equivalent digital model*. A number of detailed analyses in digital circuits([1], [4], [8]–[11]) have been reported ([11]–[13]). The inverteroperating in a strong inversion is known. The width of the PMOS must be 2-3 times width of the NMOS [1] (symmetricaltransfer characteristics). However, this setting may not suit inanalog circuits.

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In the article, the inverter design for voltage converters is discussed in order to minimize the average cross current duringthe period of the clock signal. Using BSIM model equations,an analytical description of DC characteristics ([1], [4]) will be found for this purpose. The strong inversion region is expected in the high-voltage circuits, where the behavior of the MOSFET models for analog structured design is correct. Consequently, it is not necessary to admit a specified technology, because the EKV parameters are extracted from the curves simulated using the BSIM models [3].

II. BSIM MODEL EQUATION

A real model of the MOSFET, like BSIM involves manyeffects [2]. It contains many model parameters and any derivation is very difficult (implicit form, solving of irrational equations, etc.). The static model of MOSFET is discussed as introduced in the previous text.

For MOSFET operation in high-voltage circuits where $V_{GS} \ll V_{TH}$, the following conditions must be true:

- long channel MOSFET
- strong inversion region.

Channel length is an important parameter because of the breakdown voltage. The electrical field in a structure induced by an applied voltage must be significantly less than the critical electrical field, $E = \frac{V}{L_{eff}} \leq E_{crit}$, where L_{eff} is effective channel length. A critical electrical field is limited to the valuegiven by a semi-empiric model [2].

The effective channel length is relative to the applied voltage *Vmax* (gate-source, drain-source) defined as

$$L_{eff} \gg V_{max} \frac{\mu_{eff}}{2v_{sat}}, \qquad (1)$$

where $v_{sat}$is the saturation velocity (model parameter) and $\mu_{eff}$is effective mobility.

A drain current model is given by a single equation [2]. The transition from triode to the saturation region is ensured through an effective drain-source voltage.

$$V_{DSeff} = \begin{cases} V_{DS}, & \text{for triode region} \\ V_{DSsat}, & \text{for saturation region} \end{cases} \qquad (2)$$

and for long channel MOSFET's, the saturation drain current $V_{DS} = V_{DSsat}$is given by:

$$I_{Dsat0} = \frac{1}{2}\frac{W}{L} c_{oxe} \mu_{eff} V_{DSsat}(V_{GS} - V_{TH}), \qquad (3)$$

where c_{oxe} is the electrical oxide capacitance. The boundary between the triode and saturation regions is predicted by the voltage (V_{GS}- V_{TH}) and applies a bias voltage effect and further model parameters (channel length and width...) included in

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the bulk-charge equation [2], labeled A_{bulk}. A_{bulk} is closed to unity for relatively high source-bulk bias voltage. In the other words,

$$V_{DSsat} = \frac{V_{GS} - V_{TH}}{A_{bulk}} \approx V_{GS} - V_{TH} \text{ for } V_{SB} > V_{GS}. \quad (4)$$

Generally, the output I-V curve in the saturation region(V_{DS}> V_{DSsat}) is written by several physical mechanisms.Nevertheless, considering the condition (1) short channel effect- channel length modulation (CLM) and Substrate CurrentInduced Body Effect (SCBE) can be neglected. Then the draincurrent increases linearly with the V_{DS} voltage. The slope ofthe output characteristics is mainly determined by Early voltage V_{ADIBL} due to the drain-induced barrier lowering (DIBL) effect ([1], [2], [5]). V_{ADIBL} is directly proportional to thevoltage V_{GS}, as is shown bellow. Moreover, the equation (5)contains the model parameters PDIBLC2 and PDIBLCB [2].

$$V_{ADIBL} = \frac{1}{2}\frac{V_{GS} - V_{TH}}{\text{PDIBLC2}\,(1 - \text{PDIBLCB}\,V_{SB})} \quad (5)$$

The complex drain current equation may be expressed by the formula

$$I_{Dsat} = I_{Dsat0}\left(1 + \frac{V_{DS} - V_{DSsat}}{V_{ADIBL}}\right) \quad (6)$$

for $V_{DS} \geq V_{DSsat}$.

The drain current in the triode region is a function of theV_{DS} voltage (V_{GS} = const.). The maximum of the parabolicfunction I_{DS0} =f(V_{DS}) corresponds to the voltage V_{DSsat}because of the neglected CLM mechanism ([1], [2], [5]). Then,the relationship between the drain-source voltage V_{DS} and thesaturation drain current I_{Dsat0} [5] can be written simply as

$$I_{DS0}(V_{DS}) = -\frac{I_{Dsat0}}{V_{DSsat}^2}V_{DS}^2 + \frac{I_{Dsat0}}{V_{DSsat}}2V_{DS} \quad (7)$$

for $V_{DS} < V_{DSsat}$.

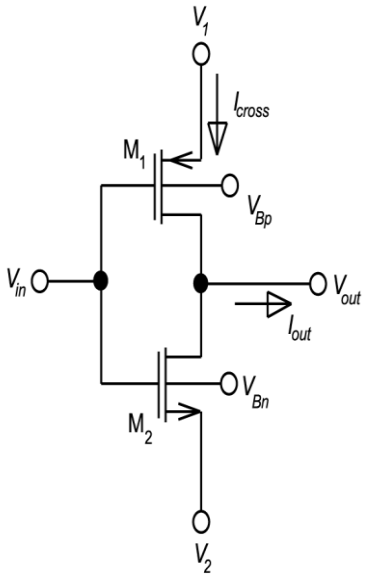
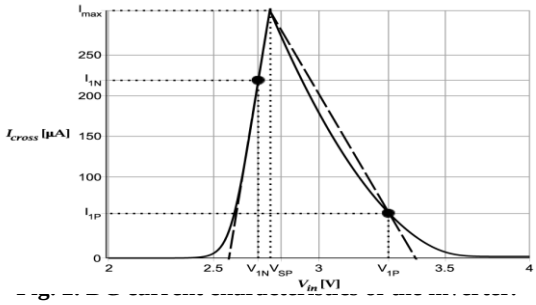


Fig. 1. The CMOS inverter.



III. STATIC PARAMETERS OF THE CMOS INVERTER

A diagram of the CMOS inverter schematic is shown in Fig. 1. All voltages are referenced to the *ground* and $V_1 - V_2 > V_{THN} + |V_{THP}|$.

The inverter´s cross current characteristics is shown in Fig. 2. A general form of the analytical expression of the cross current is divided into the three cases:

$$I_{cross} = \begin{cases} I_{DsatN}|V_{GS} = V_{in} - V_2, & \text{for C1} \\ I_{DsatP}|V_{SG} = V_1 - V_{in}, & \text{for C2} \\ 0, & \text{otherwise,} \end{cases} \quad (8)$$

C2 is: $V_{SP} \leq V_{in} \leq V_1 - |V_{THP}|$.

Cross current is maximal at the switching point V_{in} = V_{SP},see [1]. Both transistors M_1 and M_2 are in the saturationregion (Eq. 6) for this case and the drain current of eachMOSFET must be equal:

$$A_{bulk0}(V_{SB}) = A_{bulk}|_{(V_{GS}-V_{TH})_{eff}=0} \quad (9)$$

if the output current (see Fig. 1) is zero ($I_{out} = 0$). Equation(9) is more than third order for variable V_{SP}, thus simplifyingpreconditions will be introduced.

Firstly, Early voltage (Eq. 5) limits to infinity, wherefromit is compared $I_{Dsat0N} \approx I_{Dsat0P}$. Secondly, the absolutelyvalue of the drain currents of the PMOS and NMOS transistors for the derivation V_{SP} are not important; only trans conductance is important. The slope of the cross current characteristics on each interval is mainly given by the linear part of the voltage V_{GS}- V_{TH}(V_{SB})(MOS trans conductance in strong inversion is a linear function of the gate-sourc evoltage), while other powers at that voltage are not taken into account. Hence, the bulk charge equation [2] is adjusted to

and with the effective mobility substituted into the equation(3) at zero bias voltages. Finally, the formula of the switchingpoint for the BSIM model [1] can be expressed in the modifiedform:

$$V_{SP} = \frac{V_1 - |V_{THP}(V_{BS})| + \sqrt{R\frac{a}{b}}[V_2 + V_{THN}(V_{SB})]}{1 + \sqrt{R\frac{a}{b}}}, \quad (10)$$

where $a = \frac{c_{oxeN}\mu_{effN}|_{V_{GS}=V_{SB}=0}}{A_{bulk0N}|_{V_{SB}=0}}$, $b = \frac{c_{oxeP}\mu_{effP}|_{V_{SG}=V_{BS}=0}}{A_{bulk0P}|_{V_{BS}=0}}$ and $R = \frac{W_n}{L_n}\frac{L_p}{W_p}$.

or the calculation of DC power because of the discontinuous cross current characteristics at that point, as it is shown in Fig. 2. The typical characteristics of the dependence of the switching

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point on the ratio dimensions of bothtransistors is shown in Fig. 3.

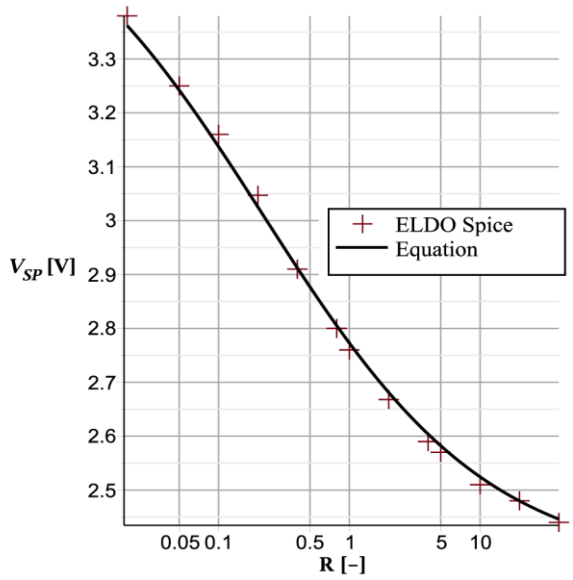

Fig. 3. Switching point analysis – dependence on the ratio *R*

Static power during the inverter´s output voltage crossing between logic 1 and logic 0 is defined as

$$P_{DC} = \int_{V_2}^{V_1} I_{cross}(V_{in})\,\mathrm{d}V_{in} = \int_{V_2+V_{THN}}^{V_{SP}} I_{DsatN}(V_{in})\,\mathrm{d}V_{in} + \int_{V_{SP}}^{V_1-|V_{THP}|} I_{DsatP}(V_{in})\,\mathrm{d}V_{in}. \quad (11)$$

The solution of equation (11) exists, but it is confusing and unnecessary for the estimation of the power dissipation.Results of the numeric integration of equation (11) shows that function is primarily determined by the function arctan[1],that *can be approximated by its argument (linear function) at zero* $\lim_{x\to 0}\left(\frac{\arctan(x)}{x}\right) = 0$. A simpler approach is based onan approximation of the characteristics (Fig. 1) in intervals $V_{in} \in \langle V_2 + V_{THN}, V_{SP}\rangle$ and $V_{in} \in \langle V_{SP}, V_1 + |V_{THP}|\rangle$ by*linear interpolation* for two points at each interval:

At the point where $|V_{GS}|$ is greater than the threshold voltage $|V_{TH}|$ (strong inversion region), the transistor is operating at the edge of the saturation region(M_1 for $V_{in} \in \langle V_{SP}, V_1 + |V_{THP}|\rangle$ and $M_2$for $V_{in} \in \langle V_2 + V_{THN}, V_{SP}\rangle$), where the drain current is approximately the linear function of the gate-source voltage. It means that quadratic part of V_{GS} voltage from expression$(V_{GS}\text{-}V_{TH})^2$ must be less than its linear part. Assumingthe equality of these parts, two solutions exists. Thefirst one is $V_{GS} = 0$ that is ignored and the second is $V_{GS} = 2|V_{TH}|$[2]:

$$I_1 = \begin{cases} I_{1N} = I_{Dsat0N}|_{V_{GS}=V_{1N}=2V_{THN}}, & \text{for NMOS} \\ I_{1P} = I_{Dsat0P}|_{V_{SG}=V_{1P}=2|V_{THP}|}, & \text{for PMOS} \end{cases}$$

thence, new formula for cross current characteristics can be expressed as

$$\tilde{I}_{cross} \approx \begin{cases} I_{1N}\frac{V_{SP}-V_{in}}{V_{SP}-V_2-2V_{THN}} + I_{max}\frac{V_2+2V_{THN}-V_{in}}{V_2+2V_{THN}-V_{SP}}, & \text{for C1} \\ I_{1P}\frac{V_{SP}-V_{in}}{V_{SP}-V_1+2|V_{THP}|} + I_{max}\frac{V_1-2|V_{THP}|-V_{in}}{V_1-2|V_{THP}|-V_{SP}}, & \text{for C2} \\ 0, & \text{otherwise,} \end{cases} \quad (12)$$

where condition C1 is: $V_2 + V_{THN} \leq V_{in} \leq V_{SP}$ and C2is: $V_{SP} < V_{in} \leq V_1 - |V_{THP}|$. The equation (12) allows to calculate the static power as the triangle area:

$$\tilde{P}_{DC} \approx \frac{1}{2} I_{max}\left(\frac{I_{max}(V_1 - 2|V_{THP}|) - I_{1P}V_{SP}}{I_{max} - I_{1P}} - \frac{I_{max}(V_2 + 2V_{THN}) - I_{1N}V_{SP}}{I_{max} - I_{1N}}\right). \quad (13)$$

[1]Analytical expression is given by the sum of the functions *arctan* and *ln*.

[2]This value is also included in the coefficient at the *arctan* in the solutionof Eq. (11).

The average current during the transition between both the logic levels is the coinciding DC power divided by the power supplyvoltage:

$$I_{av} = \frac{P_{DC}}{V_1 - V_2}. \quad (14)$$

IV. SIMULATION RESULTS

The DC parameters of the CMOS inverter were simulatedby ELDO. The simulation circuit parameters are shown inTab. I. The dependence of the average cross current (Eq. 14)on the width of the PMOS (W_p) or NMOS (W_n) transistorwas analyzed at the fixed channel lengths L_n, L_p. These weredetermined based on the condition (1), respecting the value ofthe bis voltages, as it is shown in Table I.

Analysis results in Tab. II show that an effective reduction ofI_{av} is achieved when $R \gg R_{Cmax}$ (solution R_{opt1} of Eq. 18),consequently $W_n \gg W_p$ and V_{SP} approach the lower limit,$V_{SP} \to V_2 + V_{THN}$. This is physically caused by a greatermobility of electrons in the NMOS structure compared to themobility of holes in the NMOS dimensions. Otherwise, when$R \ll R_{Cmax}$, a very large disproportion between sizes of bothtransistors adversaly affects other properties of the inverter(transistors area, dynamic properties,...), as is shown bellow. Of course, the mean value of the cross current is not only a function of R, but depends on the specific value ofW_n/L_n, W_p/L_p respectively, as is shown in Fig. 5. Thespecific sizes of the NMOS and PMOS transistors can be setby additional application requirements (time delay, switchingcharacteristics), but the ratio R must be retained. *Experience says that the optimal value of the parameter* δ is 0:4 ÷ 0:6(*Eq. 16) for practical design*. Values of the ratio R and theaverage cross current I_{av} for this range of the δ parameter arebold in Tab. II.

However, the optimal setting of R may not be optimal for the design of an inverter operating in digital circuits, where the switching point (Eq. 10) should be closed to the ideal valueof half of the supply voltage. Therefore

$$R|_{V_{SP}=V_{DD}/2} = \frac{b}{a}\left[\frac{V_1 - V_2 - 2|V_{THP}(V_{BS})|}{V_1 - V_2 - 2V_{THN}(V_{SB})}\right]^2 \quad (15)$$

and corresponding sensitivity is about 0.98 and simulated I_{av} value is about ten times higher compared to the optimizationprocess. The width of the PMOS transistor is sized to 2 ÷ 3 the width of the PMOS [1] transistor (lengths

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Volume 10, Issue 3, September 2020

are the same),provided that $V_{THN} \approx |V_{THP}|$. This condition can not be satisfied in voltage convertors due to a different supply voltageV_1, V_2in each of the convertor´s stages and the different threshold voltage of each of the transistors (body effect, [1]–[5]).

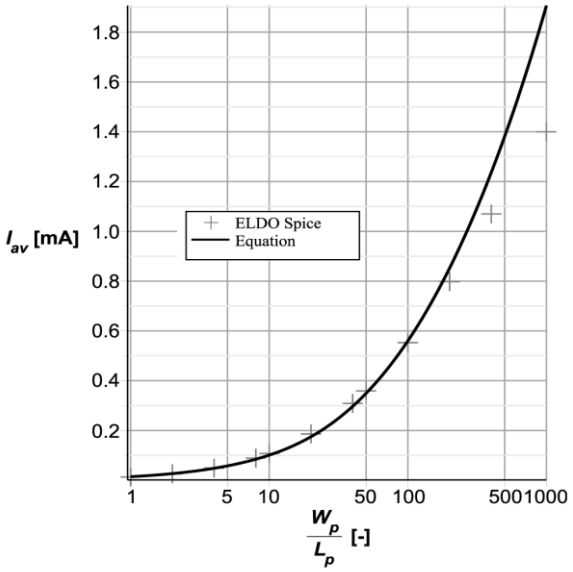

Fig. 5. Cross current vs. the W_p/L_p ratio

V. CONCLUSION

The sensitivity analysis of the switching point to the sizing of the transistors (Fig. 4) shows that it is possible to find the optimal ratio$R=\frac{W_n}{L_n}\frac{L_p}{W_p}$, while keeping a relatively big ratio *W/L* value of each of the NMOS and PMOS transistors. It is very favorable from a time response perspective. The formulae derived in this paper are applicable to the other MOSFET models including the parameters for the specified technology process. Important implications of the optimization process can be summarized in the following items:

- Asymmetric DC characteristics; switching point is notequal to the half supply voltage. It is not an appropriate configuration in a digital circuit (rise time versus fall time,noise margine for high versus low logic level,...), while these properties are not meaningful in analog ciruits. This fact has not been solved yet.
- Propagation delays between logic levels should be short because of the possibility of setting small effective switching resistances (large width) of the NMOS and PMOS. Propagation delays are not the same.
- The cross current is very small if the operating point of the inverter is set to the linear region of the voltage transfer characteristics in comparison with cross current of the ”symetrical” inverter of the same area.
- Static and dynamic properties are in sensitive to the dimensional tolerance of the transistors. The sensitivity of the proposed inverter switching point to the transistors sizing is always less than sensitivity of the inverter for digital circuit applications. It follows from the principle of the design process. All proposals were validated by the real circuit simulations.

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