Abstract—This paper presents a portrayal of the prevailing qualities of the CMOS inverter, which is utilized for voltage converters—charge siphons applications. This circuit controls transport charge between primary capacitors to make a higher DC voltage. The critical aspect of the siphon misfortunes is brought about by the inverter cross current. This current courses through the inverter on the move state and releases the capacitor, accordingly diminishes the siphon voltage gain. The CMOS inverter configuration depends on the simple square depiction for high-voltage coordinated circuits utilizing BSIM model conditions. The main advantage of this paper is to derive and investigative connection between width and length of the NMOS and PMOS semiconductors to accomplish the static force minimization. The determination has been performed dependent on the affectability examination. The quality of the proposed circuit has been confirmed by reenactment in ELDO Spice. Examination results show that the cross current is diminished by multiple times in correlation with the estimation of the standard advanced inverter (with balanced voltage move qualities). This improvement was accomplished while keeping moderately enormous region of the two semiconductors fulfilling the dynamic properties.

Index Terms—CMOS inverter, BSIM model, high-voltage, sensitivity.

I. INTRODUCTION

A CMOS inverter is a basic block (Fig. 1) for digital design circuits which performs a logic operation from A to A. However, there are also applications in the analog domain; both continuous–time circuits (oscillators, amplifiers) and discrete–time analog circuits (voltage converters). Although discrete–time analog circuits seem to be digital circuits from a system perspective, the internal state of the system is time continuous during each period of the clock signal. Results of the transient analysis show that the dominant part of losses in chargers is caused by a DC cross current that flows through inverter operating in the linear region of voltage transfer characteristics. This is undesirable because the cross current greatly decreases a pump’s voltage gain while losses caused by propagation delays of the inverter are very small.

Current research deals with the dynamic behavior of the inverter and transistor sizing, which is based on the equivalent digital model. A number of detailed analyses in digital circuits[1], [4], [8]–[11] have been reported ([11]–[13]). The inverter operating in a strong inversion is known. The width of the PMOS must be 2–3 times width of the NMOS [1] (symmetrical transfer characteristics). However, this setting may not suit in analog circuits.

In the article, the inverter design for voltage converters is discussed in order to minimize the average cross current during the period of the clock signal. Using BSIM model equations, an analytical description of DC characteristics ([1], [4]) will be found for this purpose. The strong inversion region is expected in the high-voltage circuits, where the behavior of the MOSFET models for analog structured design is correct. Consequently, it is not necessary to admit a specified technology, because the EKV parameters are extracted from the curves simulated using the BSIM models [3].

II. BSIM MODEL EQUATION

A real model of the MOSFET, like BSIM involves many effects [2]. It contains many model parameters and any derivation is very difficult (implicit form, solving of irrational equations, etc.). The static model of MOSFET is discussed as introduced in the previous text.

For MOSFET operation in high-voltage circuits where $V_{GS} \ll V_{TH}$, the following conditions must be true:

- long channel MOSFET
- strong inversion region.

Channel length is an important parameter because of the breakdown voltage. The electrical field in a structure induced by an applied voltage must be significantly less than the critical electrical field, $E = \frac{V}{L_{eff}} \leq E_{cr}$, where $L_{eff}$ is effective channel length. A critical electrical field is limited to the value given by a semi-empirical model [2].

The effective channel length is relative to the applied voltage $V_{max}$ (gate-source, drain-source) defined as

$$L_{eff} \gg V_{max} \frac{\mu_{eff}}{2V_{sat}}$$

where $\mu_{is}$ is the saturation velocity (model parameter) and $\mu_{is}$ effective mobility.

A drain current model is given by a single equation [2]. The transition from triode to the saturation region is ensured through an effective drain-source voltage.

$$V_{DS} = \begin{cases} V_{DS} & \text{for triode region} \\ V_{DSsat} & \text{for saturation region} \end{cases}$$

and for long channel MOSFETs, the saturation drain current $V_{DS} = V_{DSsat}$ is given by:

$$I_{DSsat} = \frac{1}{2} \frac{W}{L} \mu_{opt} \frac{V_{DSsat}(V_{GS} - V_{TH})}{V_{GS} - V_{TH}}$$

where $\mu_{opt}$ is the electrical oxide capacitance. The boundary between the triode and saturation regions is predicted by the voltage ($V_{opt}$, $V_{opt}$) and applies a bias voltage effect and further model parameters (channel length and width...) included in the bulk-charge equation [2], labeled $A_{bulk}$ $A_{bulk}$ is closed to unity for relatively high-source bulk bias voltage. In the other words,

$$V_{DSsat} = \frac{V_{GS} - V_{TH}}{A_{bulk}} \approx V_{GS} - V_{TH} \text{ for } V_{SB} > V_{GS}.$$
Generally, the output I-V curve in the saturation region \( V_{DS} \geq V_{DSat} \) is written by several physical mechanisms. Nevertheless, considering the condition (1) short channel effect - channel length modulation (CLM) and Substrate CurrentInduced Body Effect (SCBE) can be neglected. Then the drain current increases linearly with the \( V_{DS} \) voltage. The slope of the output characteristics is mainly determined by Early voltage \( V_{ADIBL} \) due to the drain-induced barrier lowering (DIBL) effect ([1], [2], [5]). \( V_{ADIBL} \) is directly proportional to the voltage \( V_{GS} \), as is shown below.

Moreover, the equation (5) contains the model parameters PDIBLC2 and PDIBLCB [2].

\[
V_{ADIBL} = \frac{1}{2} \frac{V_{GS} - V_{TH}}{PDIBLC2 (1 - PDIBLCB V_{GB})} \quad (5)
\]

The complex drain current equation may be expressed by the formula

\[
I_{DS0}(V_{DS}) = -\frac{I_{Dsat0} V_{DS}}{V_{DSat}} + \frac{I_{Dsat0}}{V_{ADIBL}} 2V_{DS} \quad (6)
\]

for \( V_{DS} \geq V_{DSat} \).

The drain current in the triode region is a function of the \( V_{DS} \) voltage (\( V_{GS} = \) const.). The maximum of the parabolic function \( I_{DS0}(V_{DS}) \) corresponds to the voltage \( V_{DSat} \) because of the neglected CLM mechanism ([1], [2], [5]). Then, the relationship between the drain-source voltage \( V_{DS} \) and saturation drain current \( I_{Dsat0} \) can be written simply as

\[
I_{Dsat0}(V_{DS}) = \frac{I_{Dsat0}}{V_{DSat}} V_{DS}^2 \quad (7)
\]

for \( V_{DS} \geq V_{DSat} \).

III. STATIC PARAMETERS OF THE CMOS INVERTER

A \( I_{Dest} \) for \( V_{DS} = V_{GS} \) is shown in Fig. 1. All voltages are referenced to the ground and \( V_{1} - V_{2} > V_{THP} + |V_{THN}| \).

The inverter’s cross current characteristics is shown in Fig. 1. A general form of the analytical expression of the cross current is divided into the three cases:

\[
I_{cross} = \begin{cases} 
I_{Dest} |V_GS| &= V_{in} - V_{2} & \text{for} \ C1 \\
I_{Dest} |V_{SG}| &= V_{1} - V_{ins} & \text{for} \ C2 \\
0, & \text{otherwise}
\end{cases} \quad (8)
\]

where condition C1 is: \( V_{2} + V_{THN} \leq V_{in} \leq V_{SP} \) and C2 is: \( V_{SP} \leq V_{in} \leq V_{1} - V_{TH} \).

Cross current is maximal at the switching point \( V_{in} = V_{SP} \), see [1]. Both transistors \( M_{1} \) and \( M_{2} \) are in the saturation region (Eq. 6) for this case and the drain current of each MOSFET must be equal:

\[
A_{bulk}(V_{SP}) = A_{bulk}(V_{GS} = V_{TH} + |V_{TH}|) \quad \text{at} \quad V_{in} = V_{SP} \quad (9)
\]

if the output current (see Fig. 1) is zero \( (I_{out} = 0) \). Equation (9) is more than third order for variable \( V_{SP} \), thus simplifying preconditions will be introduced.

Firstly, Early voltage (Eq. 5) limits to infinity, wherefrom is compared \( I_{Dest0} \approx I_{DestP0} \). Secondly, the absolutely value of the drain currents of the PMOS and NMOS transistors for the derivation \( V_{SP} \) are not important; only trans conductance is important. The slope of the cross current characteristics on each interval is mainly given by the linear part of the voltage \( V_{GS} - V_{TH} \), while other powers at that voltage are not taken into account. Hence, the bulk charge equation [2] is adjusted to

\[
A_{bulk}(V_{SP}) = A_{bulk}(V_{GS} = V_{TH} + |V_{TH}|) \quad \text{at} \quad V_{in} = V_{SP} \quad (10)
\]

and with the effective mobility substituted into the equation (3) at zero bias voltages. Finally, the formula of the switching point for the BSIM model [1] can be expressed in the modified form:

\[
V_{SP} = V_{1} - |V_{THP}(V_{SB})| + \frac{\sqrt{R^2 + [V_{2} + V_{THN}(V_{SB})]^2}}{1 + \sqrt{R^2}} \quad (10)
\]

where \( a = \frac{\zeta_{eff} |\tau_{eff}| V_{GS} = V_{GB} = 0}{A_{bulk} (V_{GB} = 0)} \), \( b = \frac{\zeta_{eff} |\tau_{eff}| V_{GS} = V_{GB} = 0}{A_{bulk} (V_{GB} = 0)} \) and \( R = \frac{V_{in} I_{P} L_{n}}{W_{n}} \).

The switching point is an important parameter for the calculation of DC power because of the discontinuous cross
current characteristics at that point, as it is shown in Fig. 2. The typical characteristics of the dependence of the switching point on the ratio dimensions of both transistors is shown in Fig. 3.

Static power during the inverter’s output voltage crossing between logic 1 and logic 0 is defined as

\[ P_{DC} = \frac{V_1}{V_0} \int I_{cross} (V_{in}) \, dV_{in} = \frac{V_{OP}}{V_{OL}} \int I_{sat} (V_{in}) \, dV_{in} + \frac{V_{SP}}{V_{THP}} \int I_{DR} (V_{in}) \, dV_{in} \quad (11) \]

The solution of equation (11) exists, but it is confusion and unnecessary for the estimation of the power dissipation. Results of the numeric integration of equation (11) shows that function is primarily determined by the argument function \( \tan^{-1} \left( \frac{x}{a} \right) \), that can be approximated by its argument function at zero limit, \( \lim_{x \to 0} \left( \frac{\arctan x}{x} \right) = 1 \). A simpler approach is based on approximation of the characteristics (Fig. 1) in intervals \( V_{in} \in [V_2 + V_{THN}, V_{SP}] \) and \( V_{in} \in [V_{THP}, V_{sp}] \) by linear interpolation for two points at each interval:

At the point where \( V_{CS} \) is greater than the threshold voltage \( V_{THp} \) (strong inversion region), the transistor is operating at the edge of the saturation region \( (M_f, \text{for } V_{in} \in (V_2 + V_{THN}, V_{SP})) \) and \( M_s \) for \( V_{in} \in (V_2 + V_{THN}, V_{SP}) \), where the drain current is approximately linear function of the gate-source voltage. It means that quadratic part of \( V_{GS} \) voltage from expression \( (V_{GS} - V_{TH})^2 \) must be less than its linear part. Assuming the equality of these parts, two solutions exists. The first one is \( V_{GS} = 0 \) that is ignored and the second is \( V_{GS} = 2V_{TH} \):

\[ I_1 = I_{max} \frac{V_{GS} - V_{TH}}{V_{GS} - V_{TH}} \quad \text{for NMOS} \]
\[ I_1 = I_{max} \frac{V_{GS} - V_{TH}}{V_{GS} - V_{TH}} \quad \text{for PMOS} \]

hence, new formula for cross current characteristics can be expressed as

\[ I_{cross} \approx \begin{cases} \frac{1}{2} I_{max} \left( V_{max} - 2V_{TH} \right) - I_{LP} V_{SP} - I_{SP} V_{TH} & \text{for } C1 \\ 0 & \text{otherwise} \end{cases} \quad (12) \]

where condition C1 is: \( V_2 + V_{THN} \leq V_{in} \leq V_{SP} \) and C2 is: \( V_{SP} \leq V_{in} \leq V_2 + V_{THP} \). The equation (12) allows to calculate the static power as the triangle area:

\[ I_{av} = \frac{P_{DC}}{V_1 - V_2} \quad (14) \]

IV. SIMULATION RESULTS

The DC parameters of the CMOS inverter were simulated by ELDO. The simulation circuit parameters are shown in Tab. I. The dependence of the average cross current (Eq.14) on the width of the PMOS \( (W_p) \) or NMOS \( (W_n) \) transistor was analyzed at the fixed channel lengths \( L_n, L_p \). These were determined based on the condition (1), respecting the value of the bias voltages, as it is shown in Table I.

Analysis results in Tab. II show that an effective reduction of \( I_{av} \) is achieved when \( R \gg R_{Cmax} \) (solution \( R_{opt} \) of Eq. 18), consequently \( W_n \gg W_p \) and \( V_{SP} \) approach the lower limit, \( V_{SP} \rightarrow V_2 + V_{THN} \). This is physically caused by a greatemobility of electrons in the NMOS structure compared to the mobility of holes in the NMOS dimensions. Otherwise, when \( R \ll R_{Cmax} \), a very large disproportion between sizes of both transistors adversely affects other properties of the inverter (transistors area, dynamic properties,...), as is shown bellow. Of course, the mean value of the cross current is not only a function of \( R \), but depends on the specific value of \( W_n/L_n, W_p/L_p \) respectively, as is shown in Fig. 5. The specific sizes of the NMOS and PMOS transistors can be set by additional application requirements (time delay, switching characteristics), but the ratio \( R \) must be retained.

Experience says that the optimal value of the parameter \( \delta \) is \( 0.4 \pm 0.6 \) (Eq. 16) for practical design. Values of the ratio \( R \) and the average cross current \( I_{av} \) for this range of the parameter are bold in Tab. II.

However, the optimal setting of \( R \) may not be optimal for the design of an inverter operating in digital circuits, where the switching point (Eq. 10) should be closed to the ideal value of half of the supply voltage. Therefore

\[ R = \frac{P_{DC}}{b a} \left( \frac{V_1 - V_2 - 2V_{TH} \left( V_{BS} \right)}{V_1 - V_2 - 2V_{TH} \left( V_{SD} \right)} \right)^2 \quad (15) \]
and corresponding sensitivity is about 0.98 and simulated $I_{in}$ value is about ten times higher compared to the optimization process. The width of the PMOS transistor is sized to $2 + 3$ the width of the PMOS [1] transistor (lengths are the same), provided that $V_{THS} \leq V_{THP}$. This condition can not be satisfied in voltage converters due to a different supply voltage $V_r$, $V_{in}$ in each of the converter’s stages and the different threshold voltage of each of the transistors (body effect, [1]–[5]).

![Graph showing cross current vs. the W/L ratio](image)

**Fig. 5. Cross current vs. the W/L ratio**

## V. CONCLUSION

The sensitivity analysis of the switching point to the sizing of the transistors (Fig. 4) shows that it is possible to find the optimal ratio $W/L = \frac{W_n}{L_n} \Rightarrow \frac{W_p}{L_p}$ while keeping a relatively big ratio $W/L$ value of each of the NMOS and PMOS transistors. It is very favorable from a time response perspective. The formulae derived in this paper are applicable to the other MOSFET models including the parameters for the specified technology process. Important implications of the optimization process can be summarized in the following items:

- Asymmetric DC characteristics; switching point is not equal to the half supply voltage. It is not an appropriate configuration in a digital circuit (rise time versus fall time, noise margin for high versus low logic level,...), while these properties are not meaningful in analog circuits. This fact has not been solved yet.
- Propagation delays between logic levels should be short because of the possibility of setting small effective switching resistances (large width) of the NMOS and PMOS. Propagation delays are not the same.
- The cross current is very small if the operating point of the inverter is set to the linear region of the voltage transfer characteristics in comparison with cross current of the "symmetrical" inverter of the same area.
- Static and dynamic properties are sensitive to the dimensional tolerance of the transistors. The sensitivity of the proposed inverter switching point to the transistors sizing is always less than sensitivity of the inverter for digital circuit applications. It follows from the principle of the design process. All proposals were validated by the real circuit simulations.

## REFERENCES


