Minimization of Jitter in Digital Systems using Dual Phase-locked Loops

A. Telba, J. M. Noras

Abstract—Timing jitter is a concern in high-frequency timing circuits. Its presence can degrade system performance in many high-speed applications. This paper describes a new method for minimization of timing jitter using two phase-locked loops connected in cascade, where the first one has a voltage-controlled crystal oscillator to eliminate the input jitter and the second is a wide-band phase-locked loop. RMS jitter, the usual system performance criterion, is analyzed in both phase-locked loops, and results of simulations using MATLAB are presented. The methodology described is also applicable to other types of clock generator.

Index Terms—Jitter, Oscillator Noise, Oscillator Stability, Phase Jitter, Phase-Locked Loops, Phase Noise, Voltage Controlled Oscillators.

I. INTRODUCTION

Phase-locked Loop (PLL) technology is used in a wide range of applications including modern data communication and wireless communications. Computer-related applications abound, including microprocessors, data busses, video and audio ICs. As the speed of microprocessors approach and exceed 5 GHz, and serial data transmission rates approach and exceed 10 Gb/s, the difficulties and complexities of designing and manufacturing a PLL for use at these speeds become severe. An important problem in PLL design and manufacturing is to simulate, measure, and verify loop response and noise processes in order to satisfy goals of time and frequency domain response, as well as good noise and jitter performance. In this paper, we introduce a novel methodology that is capable of simulating PLL loop response and noise-jitter processes. The most important use of PLL circuits is to recover the clock from a given data stream [1]-[3]. Data coming into the recovering circuit have jitter at the Voltage Controlled Oscillator (VCO) input due to inter-symbol interference and other undesirable real-world effects such as power supply noise, component tolerance and any other general noise. This means that the received data edges (for example zero-crossings) do not happen at fixed time intervals but vary around the ideal. The PLL, being a narrow-band system, will tend to average out these variations and produce a clock which is closer to the ideal. However, the clock recovery PLL must be able to track any jitter in the lower frequency ranges so that no data is lost, and the amount of jitter here can be quite large. The ability of the PLL to retiming the incoming data correctly despite jitter is called jitter tolerance. In addition, a narrow-band PLL may not be able to lock on to the incoming frequency since the capture range (the range of frequencies over which the PLL can make the oscillator frequency equal the reference frequency) is a direct function of the bandwidth.

II. JITTER ANALYSIS AND SIMULATION

Jitter can be classified as timing jitter, period jitter and long term (or accumulation) jitter [4], where long term jitter is defined as the deviation of the clock over multiple cycles. In comparison, period jitter is defined for one clock cycle. Due to its random nature, this jitter can be quantified with peak-to-peak or Root Mean Square (RMS) parameters. Defining the clock rising-edge crossing point at the threshold \( V_{TH} \) as \( T_{PER}(n) \) and \( n \) as the time domain index, period jitter, \( J_{PER} \), shown in Fig. 1, can be expressed as:

\[
J_{PER} = T_{PER}(1) - T_o
\]  

(1)

Where \( T_o \) is the period of the ideal clock cycle. Since the clock frequency is constant, the random quantity \( J_{PER} \) must have a zero mean. So, \( J_{PER} \) (RMS) can be calculated by:

\[
J_{PER}^{(RMS)} = \sqrt{J_{PER}^2}
\]  

(2)

From the relation between RMS period jitter and phase noise using the Fourier series expansion, it is clear that a square-wave clock signal has the same jitter behavior as its base harmonic sinusoid signal [4-6]. This property makes the jitter analysis of a clock signal much easier. According to [4], the RMS jitter can be expressed as follows:

\[
J_{PER}^{(RMS)} = \frac{1}{2\pi f_c}\sqrt{\int_{0}^{T_c} \frac{\Theta^2(t)}{2\pi f_c} dt}
\]  

(3)

and the period jitter is:

\[
J_{PER} = \frac{\Theta(t)}{2\pi f_c}
\]  

(4)

From Eq.4, the sinusoid signal is phase modulated by the phase noise \( \Theta(t) \), so the phase noise is always much smaller than \( \pi/2 \). In applications such as SONET and generally with high bit rates, the RMS jitter can be calculated over the bandwidth from \( f_1 \) to \( f_2 \) as follows:
The relation between RMS jitter and noise power is given by:

\[
J_{\text{PER}(\text{RMS})} = \frac{1}{2\pi f_c} \sqrt{\int_{-f_c}^{f_c} \frac{1}{2} \left( \frac{x(t)}{f(t)} \right)^2 df}
\]  \hspace{1cm} (5)

In this paper, a prototype system is developed, with analysis and processing as shown in Fig.2, using a Simulink block diagram model in order to produce a jittered signal. The procedure uses a sinusoidal signal with added random noise that can produce jitter when applied to a zero-crossing circuit with defined saturation levels, where the jitter of the output signal will depend on the added noise power. The jitter level can be measured using the M-file block shown in Fig.2. From the simulation results of this jitter measurement setup, it was found that the RMS jitter increases as the noise power increases, with higher slope above 10^6 µW noise power as shown in Fig 3.

**Fig.2 Setup for Jitter Generation and Measurement**

**III. JITTER REDUCTION TECHNIQUES**

Different techniques have been reported for the design and implementation of de-jitter circuits or low jitter clock recovery circuits, for example, modifying the filter design to narrow the PLL bandwidth and make the phase noise at the VCO input as low as possible [7]-[8], reducing power supply noise [9]-[11], eliminating ground bounce [11], using a voltage-controlled crystal oscillator (VCXO) [7],[12], a dual phase frequency detector [13] and a charge pump as a phase frequency detector [14]. An example of a de-jitter PLL circuit is shown in Fig.4. This circuit is designed to generate a stable, low-jitter clock based on either the recovered received clock or the transmit clock input [7], but a problem with this design is that it requires a VCXO that has the same reference frequency. To avoid this problem, the proposed circuit in Fig.5 uses two cascaded PLLs, the first one using a VCXO with a center frequency \( f_i \) not necessarily equal to \( f_{in} \) as that for the above circuit (Fig.4). The second one is a narrow band PLL with wide sweep range. When the first loop is in a lock condition we may write

\[
f_{in} / N = f_i / M_1
\]  \hspace{1cm} (6)

When the second loop is in lock condition we may write:

\[
f_{out} / M_2 = f_x / N
\]  \hspace{1cm} (7)

\[
f_{out} = f_{in} (M_1 M_2 / N^2)
\]  \hspace{1cm} (8)

If we choose \( M_1=M_2=N \), then \( f_{in} = f_{out} \), independently of the value of \( f_i \). Since \( f_i \) has low jitter, as it is produced using the PLL with a VCXO, then \( f_{out} \) will keep at least this amount of jitter. On the other hand we can get more reduction in jitter by careful design of the second PLL, and the filter design in this case is relatively easy since the input signal is already partially de-jittered. Notice that narrowing the PLL bandwidth without using a VCXO is unacceptable because in this case the PLL would not be able to lock while trying to track the phase variations embedded in the signal if this was taken directly from the clock recovery circuit.

**Fig.4 Block Diagram of PLL De-Jitter Circuit**

**IV. CONCLUSION**

PLLs are used in many applications. In our case we used two PLLs in cascade to minimize the RMS jitter and get a wide band of frequencies independent of the center frequency of the VCXO while changing the dividing ratios M and N. Fig. 6 shows the relation between RMS jitter and noise power at different values of N (N=130,150,170, 193) at the input of the circuit in Fig.5, while Fig. 7 shows how the jitter at the output is correspondingly reduced. Thus, we conclude that our proposed circuit helps in minimizing the jitter. In future work, we propose to implement our design experimentally.
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