High Speed Low Power Network Processors: Efficient Power Management Techniques

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Abstract: Power consumption is the bottleneck in achieving high performance. Power dissipation needs to be looked into the various levels of the design namely: circuit level, device level, architecture level and system level. With the increase in the networking, network processors (NP) have emerged as platform providing high performance and flexible in building the routers. Its observed from the survey of previous work, the processing elements, the micro engines (ME) of the NP consumes the power more. The simulation tool for this analysis used is the NepSim. Hence, the effort is to be made in reducing the power of the MEs. This paper initially brieﬁes on the basics of power consumption in VLSI systems and the architecture of NP IXP1200. The emphasis is done on the analysis of power dissipated/consumed at the different levels of NP namely: packet level, instruction level and the architecture level. The later part of the paper wholly concentrates on the power management techniques at the architectural level. These different techniques are: clock gating, dynamic voltage and frequency scaling, power gating and very new method of designing the architecture in an asynchronous way.


I. INTRODUCTION

Network processors are the basic building blocks of today’s high-speed, high demand, quality-oriented communication networks. Designing and implementing network processors requires a new programming paradigm and an in-depth understanding of network processing requirements. Network processors (NPs) are chips—programmable devices that can process network packets (up to hundreds of millions of them per second), at wire-speeds of multi-Gbps. Their ability to perform complex and flexible processing on each packet, as well as the fact that they can be programmed and reprogrammed as required; make them a perfect and easy solution for network systems vendors developing packet processing equipment. Network systems, therefore, face an ever-increasing magnitude of packets they have to handle, while at the same time, the processing of these packets becomes more and more complex. This creates a gigantic performance problem. In order to cope with it, the traditional general purpose Central Processing Unit (CPU) in the network systems is replaced with Application Specific Integrated Circuits (ASICs), which are hardwired processing devices. However, the rapid changes in technology, dynamic customer requirements, and a pressure for time-to-market, short developing cycles and lots of revisions have become necessary. All of this has required an innovative approach toward network systems architecture and components. In today’s world, the need and the demand on high performance devices has increased exponentially. This increase has initiated driving more functionality and hence, a large no of transistors on a single chip. Hence, power consumption has become the bottle neck in achieving high performance, small size devices. This leads towards the research into low power, high speed VLSI systems. Power consumption is determined by the factors namely the [1] dynamic power, short circuit power and leakage power including the frequency, supply voltage, switching activity and capacitor. The power consumption equation is given as:

\[ P = P_{\text{dynamic}} + P_{\text{shortcircuit}} + P_{\text{leakage}} \]  

Dynamic power is also the switching power defined as:

\[ P_{\text{dynamic}} = a \times C \times V^2 \]  

In equation 2, \( a \) is the switching activity, \( C \) the capacitor, \( V \) the supply voltage and \( f \) the frequency. This power can be lowered by using multiple Vdd or dynamic Vdd control. The switching activity can be reduces using the techniques of logic optimization, gated clock and prevention of glitches. To a larger extend the frequency is not increased but the same frequency is utilized efficiently at the logic and architectural level by employing the parallel processing obtaining the same throughput at lower clock frequency. \( P_{\text{shortcircuit}} \) is the short circuit power caused by the rise and fall time of the input signal, which results in pull up and pull down networks to be ON simultaneously for a short moment. This power is the product of the short circuit current and the supply voltage. The leakage power consumption has increased with the aggressive scaling of the devices. This power is almost 30-40% of the total power consumption. The increase in the performance which means adding more functionality on a single chip gives rise to issues namely: power and thermal management, testing, memory bandwidth, fault tolerance, OS design, programming model, modeling and benchmark. Thus the research challenges are low power chip design, low power communication as communication consumes almost 35% of the power, platform development, testing and reliability and security. This paper aims at presenting the high performance network processor IXP 2XXX of Intel highlighting on what are power consumption, analysis and management concerns for the Network Processor. In this paper first, the overview of the network processor is described in section II. Focus will then be on the power
consumption and analysis at various levels in the network processor in section III. The section IV will highlight on the power management techniques at the architectural level. Section V concludes the paper.

II. NETWORK PROCESSORS (NP)

The NP is an integrated Network Processor, comprised of a single StrongARM processor, four/six/eight Microengines, standard memory interfaces, and high-speed bus interfaces. It is targeted at networking applications requiring a high degree of flexibility, programmability, scalability, performance, and low power consumption. The unique architecture of the network processor is it affords the user a highly concurrent packet processing model, while keeping the programming model simple. The key features are:
- Multi-Processing
- Distributed Data Storage architecture
- Hardware Multi-Threading
- Active Memory Optimizations
- Multi-level Concurrency
- Block Data Movement
- Scalability

The typical architecture of IXP 1200 functional units is as shown in figure 1.

III. POWER CONSUMPTION ANALYSIS

Power is the major concern in the design of the high speed VLSI architectures. Power consumption in a high speed VLSI system like NP is of two main sources: Dynamic and Static. With the increase in speed, the power consumed is increased. This is true in case of network processors. The power that is consumed is different at different levels and functional units. The function of the network processors is; getting the packet, processing it and forwards it to the next router. Hence, power that is consumed is: at architectural level, instruction level and at the packet level. NP workloads have large instruction level parallelism and data level parallelism. The power increases with the increase in the number of the MEs.

A. Architecture Level

The architecture of NP basically constitute the hardware components namely: ALU and shifter, cache structures namely queues and arbiters, ME’s command FIFO, SRAM, SDRAM etc. To find out the power consumed by each of these units the simulator NepSim [3] is used. Each ME is ON for almost all the time, implies that the power is consumed but idle. It is observed that MEs are the major power hungry component. The MEs are either receivers or transmitters. The transmitting ME’s consume more power than the receiving one. The analysis of these MEs is done for different benchmarks. The power consumed by the different functional units within the ME is as shown in the figure 2.

![Fig 1: IXP1200 Functional Block Diagram](image)

The Strong ARM core is a full 32-bit RISC processor core with integrated caches that can be used for management functions, running routing protocols, exception handling, and other tasks. There six, fully programmable Microengines (ME) are used for high-speed packet inspection, data manipulation, and data transfer. SDRAM Unit is a shared, intelligent memory interface that can be accessed by the StrongARM core, the Microengines, and devices on the PCI bus. PCI Bus Interface Unit is a standard interface that may be used to interface to other PCI devices, or another host processor. IX Bus unit is an intelligent data movement engine controlled by the Microengines that are capable of transferring blocks of data between the IXP1200 and networking devices such as MACs and SARs. The details of the architecture are explained in the reference manual [2]. The MEs have this large local data transfer register area, one Reference Command can cause a block of data to be loaded into one portion of the transfer register area, while another Reference Command can cause a block of data to be loaded into a different portion of the transfer register area, without overwriting each other. The IX Bus Transmit and Receive FIFOs serve as temporary buffer areas where IX Bus data are stored.

![Fig 2: Power Consumed By Functional Units of ME](image)
From figure 2 it can be analyzed using the NepSim simulator that ALU and the control store consume the power most. Of which ALU is the maximum. Hence, work needs to be carried out on how to reduce the power of the ALU.

**B. Instruction level**

Network Processors designed have large number of ME, which in turn process the data with multithreading to achieve the high degree of parallelism. The workloads in NP have large instruction-level parallelism and data-level parallelism. The efficient architecture also looks into the efficient design of the scheduler. The scheduler architecture can either be dynamic or static. In [4], the characterization parameters namely the performance and power dissipation of statically ILP is implemented and compared with the dynamic scheduler architecture. In dynamically scheduled architectures the power consumption of the instruction window increases with the increase in the issue width. The statically scheduled architectures demonstrate better performance and greater advantage on power.

**C. Packet level**

The packet level basically deals with the incoming of the packet, classifying it using different rules, processing it and then forwards it to the router. In [5], the five different algorithms are implemented on the power hungry programmable NP. The algorithms are: recursive flow classification (RFC), hicuts, hyper cuts, extended grid of iris and tuple space search with pruning. The analysis is tabulated in table I. These algorithms were chosen for their high speed classification, low memory usage, scalability to large subsets and low power consumption for five field subsets

<table>
<thead>
<tr>
<th>Parameters</th>
<th>RFC</th>
<th>Hicut</th>
<th>Hypercut</th>
<th>EGC-Te</th>
<th>TSS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Memory Consumption vs rule</td>
<td>Worst case Memory needed is 3MB for 191 rules</td>
<td>Matching the hyperCut</td>
<td>Best as 56KB of memory for 2191 rules 1.7KB for 60 rules.</td>
<td>Matching the hyperCut</td>
<td>High due to 65KB direct lookup and hash table</td>
</tr>
<tr>
<td>Worst case lookups (WCLU)</td>
<td>Best performer needing only 12 memory lookups for all the rule set.</td>
<td>Outperformed as it needed to access extra information when traversing the decision tree</td>
<td>Largest WCLU for rule set greater than 1000 rules</td>
<td>Maintains a constant WCLU for the whole range of ruleset</td>
<td>WCLU of 52 for 500 rules</td>
</tr>
<tr>
<td>Average energy needed to classify a packet</td>
<td>Performs best, is an average 1.46µJ to classify packet</td>
<td>10.89 µJ</td>
<td>19.2 µJ</td>
<td>Worst as it needs 76.57 µJ</td>
<td>53.25 µJ</td>
</tr>
</tbody>
</table>

**IV. POWER MANAGEMENT TECHNIQUES**

The two main sources of power dissipation in a complex VLSI system are: Dynamic and Static power dissipation. Dynamic power is due to the switching activity while the static power is due to the leakage current through the inactive transistor. This section will describe the different power management techniques at the architecture level. The different techniques are:

**A. Clock gating:**

NP has a large number of functional units and MEs. At any given time not all the units are functioning. This can be seen as an advantage to reduce power. The clock gating technique reduces dynamic power consumption by disabling the clocks for those units that are not needed currently. In [6], this technique is applied on the processing units which process the packets. It is important to know which functional units should be made inactive. This technique does not put off the power but make the unit inactive. It is equally important to reactivate them. The different policies could be: selecting the parameter, determining the threshold, terminating threads gradually, reschedule packets for threshold, avoiding extra packet loss etc., Clock gating saves power by preventing unnecessary activity in functional units and eliminates power dissipation on clock network.

**B. Dynamic Voltage and Frequency Scaling**

Dynamic voltage and frequency scaling (DVFS) is a commonly-used power-management technique where the clock frequency of a processor is decreased to allow a corresponding reduction in the supply voltage. This reduces power consumption, which can lead to significant reduction in the energy required for a computation. Dynamic power reduction is accomplished through voltage scaling. The clock frequency and supply voltage are scaled dynamically based on the workload. This technique reduces the clock speed and voltage of domains when slower performance is acceptable.

**C. Power gating**

Sub threshold leakage current is one of the sources of power consumption. A conventional way to reduce this power is to block the supply voltage from reaching the transistor referred to as power gating [7]. In this technique, switch the power for a related set of logic so that it can be turned off when not needed. Header or footer switches may be used. Switching may be fine or coarse grain. One way out is to use a header transistor [7]
to block the supply voltage from reaching a functional unit is as shown in figure 3.

![Power Gate Detection Circuit](image)

**Fig 3: Power Gating Using Header Transistor**

Fig 3 contains the power gate detection circuit, whose output is given to the gate of transistor through an inverter. This detection circuit will decide whether the power VCC is to be given to the functional unit or not.

### D. Architectural Design

The architectural design means a totally different approach in designing the NP. The approach could be either asynchronous synchronous, or dataflow architecture. The architecture can be either being a base parallel model or pipelined model. The model can be of the combination that is parallel model with pipelined capability or pipelined with parallel bus. These are the basic models [8] that one could get the details about. The earlier architectures were fixed-function ASICs, control flow multiprocessors which have their own advantages and disadvantages [9]. The dataflow architectures use the availability of data to fetch rather than the availability of instruction to fetch data. Dataflow computing describes programs as dataflow graphs and instruction as the nodes. The architecture includes the packet instruction set computer, engine access point and execution context. This architecture eliminates the need for a complex, power consuming bus, memory stalls replicated storage of packet data, branching delays etc. The synchronous or the conventional architecture consists of the microprogramed processor, next address logic and datapath. This architecture is governed by the global clock. All the computations take place with respect to the clock. Those traditionally the architectures are synchronous, asynchronous architectures can be designed which have the advantage of timing, low power dissipation, improved performance etc. The asynchronous architectures are also called the self timed architectures. Since there is no global clock, the sequence of operations is performed through the concept of handshaking. Few of the asynchronous circuits as programmable asynchronous controllers [10] were used in the data-driven machines. In [11], the design of efficient application specific asynchronous micro engines is discussed. Here the architecture uses a horizontal microcode that allows programmability of its datapath by arranging the datapath units into serial parallel cluster for each microinstruction. In all the above discussion the paper aims at optimizing the power with the required performance. Hence, the designer needs to handle scenarios by inserting extra circuitry in the design, which performs special functions like switching, retention of the data and isolation. Thus, the power management techniques require the coordination between the circuits, architectures and the simulation tools.

### V. CONCLUSION

This paper gives an insight into the high speed processing system the network processor and the low power design concepts. This paper highlights on the new aspects of designing the low power and high speed network processor. To conclude, this paper summarizes as:

- Network processor is a high speed processor used in network for the processing of the packets. The functional unit consumes more power is the Micro engine. Thus, it needs to be designed for low power.
- Power consumption takes place during the packet processing and classification. Hence, an computer engineer can look into the design of the hardware scheduler or the scheduling algorithms were the power dissipation can be reduced.
- Lastly, the paper elaborates on the different power management techniques. These can be used at the architecture level, where in the RTL coding can be done, power can be analyzed and the design can be refined. The asynchronous design of the functional units can lead to less power dissipation in the near future.

### REFERENCES


AUTHOR’S PROFILE

Roopa kulkarni received her M.Tech in VLSI Design and Embedded Systems, from Visvesvaraya Technological University, Belgaum and B.E. (E & C Engg.) from KLS’s Gogte Institute of Technology, Belgaum. Pursuing her Ph.D. in the field of Low power high speed VLSI design from Visvesvaraya Technological University, Belgaum. She has publication in national and international conferences. She has guided 20 (approx.)UG projects of which one of her project won the best project at KSCST 33rd SPP exhibition.

Dr. S.Y.Kulkarni obtained his BE degree from BVB College of Engineering and Technology, Hubli with II Rank to Karnataka University Dharwar. He did his post graduation (M.Tech) and Ph.D from a highly reputed Indian Institute of Technology, Mumbai in the current field of VLSI Design. Dr.Kulkarni has wide range of experience in both industry and academia. Dr. Kulkarni has published about 42 technical papers in National and International conference and Journals. He has chaired / co-chaired several technical sessions in International conferences and also delivered keynote addresses. His two papers have been selected for “Best paper” award. He has guided several UG and PG projects. Many projects have received “Best Project” award. He has guided 2 Ph.D students and at present he is guiding 5 Ph.D students. Dr.Kulkarni is recipient of several awards. He is awarded with Hon. Membership of Prestigious International Society for Hybrid Microelectronics (ISHM), USA and International Interconnect Material and Packaging Society (IMAPS), USA. He has also received the most prestigious JAYCEE award “Outstanding Young Indian”. He has also received the Bharatiya Vidya Bhavan National Award for Best Engineering College Principal 2009 in recognition of the outstanding contribution to the Academic Community and the Students.