A 2.45 GHz Voltage Controlled Oscillator using 0.18µm CMOS for PLL

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Abstract- This paper presents a Low power consumption & Low phase Noise Voltage Controlled Ring Oscillator (VCRO) operated at 2.45 GHz. Frequency implemented in 0.18 µm complementary metal-oxide semiconductor (CMOS) technology with the unique differential delay cell. The Voltage Controlled Ring Oscillator is design in Tanner Tool Version 13 environment. Power Consumption should be reduced to improve the performance of the VCRO. In addition to this the Ring Oscillator provides the low phase noise. The VCRO required less area than LC oscillator hence it is better to used in the circuit. The implementation of ring Oscillator in CMOS technique is easy. Due to the low power consumption & low phase noise this VCRO will be the efficient module for PLL (Phase Locked Loop).

Keywords - 2.45 GHz VCRO; CMOS; Differential; Ring oscillator; 0.18µm CMOS VCO for PLL;

I. INTRODUCTION

As the demand of portable electronic and wireless communication products increases, the attention is provide towards to make devices more portable. The Wireless communication system contains many transceivers such as low-noise amplifiers, power amplifiers, mixers, digital signal processor, filters, and phase-locked loops. Voltage controlled oscillators play a critical role in communication systems, providing periodic signals required for timing in digital circuits and frequency translation in radio frequency Circuits. While oscillators exhibit periodically time-Varying Characteristics, this dissertation is concerned with an electrical signal at a specific Frequency. When it is used for frequency translation, we often refer to an oscillator as the Local oscillator (LO). A Typical PLL is made up of a VCO, low-pass loop filter, phase detector, and frequency divider. Because the PLL is involved in frequency translation and Channel selection, its spectral purity affects the performance of an overall wireless system. The spectral purity of the PLL output depends heavily on that of the VCO. Designing voltage controlled oscillators for this monolithic integration is always desirable but most challenging. The first requirement is to achieve high frequency operation with reasonable power consumption.

However, the most critical challenge for the VCO is the phase-noise performance.

The basic block diagram of PLL containing VCO is as shown below: This PLL is composed of phase detector (PD), low pass filter (LPF), voltage controlled oscillator (VCO) and frequency divider as shown in Fig. 1. In which the most power hungry module is VCO, In the PLL the incoming communication signal is demodulated with the help of a synchronized VCO signal. A VCO output which frequency varies with respect to a reference frequency. A reference frequency is compared with the VCO output frequency, which generates an error signal. This is the control voltage for the VCO.

![Fig 1: Block diagram of PLL](image)

![Fig 2: Block Diagram of Oscillator](image)

The VCO frequency is tuned such that it will shift to the reference frequency until the error signal comes down to zero. VCO generates frequency and changes the oscillating frequency varying control voltage. Hence the low power consumption VCO improves the performance of the PLL.

An oscillator that changes its frequency according to a control voltage feed to its control input is Voltage Controlled Oscillator [13]. The most common types of Voltage Controlled oscillator are Ring oscillators and LC oscillators.
Where

\( H(s) \) is feedback function of oscillator.

The Barkhausen criteria for oscillation which govern condition for oscillators are given by

\[ H(s) \geq 1 \]  \hspace{1cm} (2)

\[ \angle H(s) = 180^\circ \]  \hspace{1cm} (3)

These conditions are necessary but may not be sufficient to ensure oscillation. A VCO is an oscillator whose open loop transfer function \( H(s) \) can be varied by a control voltage.

A Ring VCO is configured using voltage controlled feed forward inverting stages. A ring oscillator consists of multiple gain stages within the loop. Each gain stage can be as simple as an inverter, or as complicated as a differential amplifier. Whereas the LC VCO contains the inductor and capacitor, due to which it required the large area. In addition, it is very difficult to integrate inductor in digital CMOS technology [8]. This short comes of LC VCO is overcome by the ring VCO or better known as VCRO.

In this paper, a Low power consumption and low phase noise Voltage Controlled Ring Oscillator with four-stage single-delay loop is implemented in 0.18µm CMOS techniques. It operated at 2.45 GHz centre frequency. Due to the low power consumption it is vital module for the PLL.

This paper will be organized as follows: Section II discusses the details of oscillator design; Section III describes construction of delay cell and its operation; Section IV presents comparisons with other works; a conclusion is drawn in Section V.

II. DESIGN OF VCRO ARCHITECTURE

Fig 3 shows the four stages single delay path architecture. The oscillator satisfied the Barkhausen criterion. The open loop transfer function for the ring VCO is given by equation

\[ H(S) = - A_0^4 / (1 + S/W_0)^4 \]  \hspace{1cm} (4)

In this work the concentration is provide to reduce the power consumption by adjusting the supply voltage and input frequency.

The oscillation frequency of a ring VCO with \( N \) stages of identical delay cells is express in equation (4). The oscillation frequency is inversely proportional to the number of delay stages. The oscillation frequency of a ring VCO is given by [12]

\[ F_{\text{ring}} = 1 / N \cdot t_{\text{delay}} \]  \hspace{1cm} (5)

Where

\( N \) is the number of stages and

\( t_{\text{delay}} \) is the delay time for each stage.

For every signal cycle, there is a downward as well as an upward transition. Since the high-to-low (\( t_{\text{pHL}} \)) and low-to-high (\( t_{\text{pLH}} \)) propagation delays associated with these transitions are not usually equal, the average propagation delay is given by

\[ T = (t_{\text{pHL}} + t_{\text{pLH}})/2 \]  \hspace{1cm} (6)

In VCO Phase noise is the frequency domain representation of rapid, short-term, random fluctuations in the phase of a waveform, caused by time domain instabilities. An oscillator can be considered as a filtered noise generator and therefore noise will surround the carrier. The phase noise describes the fluctuation of the oscillation frequency. In the proposed VCRO by proper sizing the transistor lower down the phase noise. Due to which it is better than compared VCO model.

III. PROPOSED DELAY CELL ARCHITECTURE

In this research, novel delay cell architecture for the VCRO has been proposed as shown in Fig. 4. Additionally, it will improve output voltage stability.
serially connected PMOS with a load capacitor will be employed in parallel with each NMOS input for frequency tuning.

The operation of the delay cell can be described considering half-cell circuit. While the input, \( I_A \) will be high (near VDD), the input, \( I_B \) will be low (equal to zero volt). This will turn on NMOS of the node, \( I_A \). On the other hand, PMOS of the input node, \( I_A \) and cross coupled PMOS connected in parallel with this input PMOS will remain off. Then voltage of the output node, \( O_A \) will be grounded. During that period, charge from the capacitor (\( C_1 \)) will be discharged, or in other words, a path will be formed, which sinks current from out \( A \) to bring its potential to 0 V. Similarly, if the input, \( I_A \) will turn into 0 V, then the input, \( I_B \) will be high (near VDD). Zero potential of the input, \( I_A \) will turn on PMOS and turn off NMOS simultaneously. Cross-coupled PMOS connected in parallel with the input PMOS of the node, \( I_A \) will also remain switched on at this time. Thus, the discharged capacitor will be recharged again through these PMOS transistors. However, in both operations, a PMOS tuning transistor will control the overall charging and discharging of the load capacitor. \( V_{DD} \) is the voltage source of the circuit the inductor and capacitor VCO are difficult to integrate in CMOS techniques as well as it provide the less oscillation to the output swing. Whereas ring VCO provide the proper oscillation to the output. The delay cell using architecture is the better than other therefore the Voltage Controlled Ring Oscillator using the delay cell is also better to used in communication application.

IV. SIMULATION RESULTS

In this section we present simulation results using differential delay structure. The proposed Voltage Controlled Ring Oscillator (VCRO) is implemented in 0.18µm complementary metal oxide semiconductor (CMOS) techniques. We performed spice simulation for proposed circuit by using Tanner EDA software; we use S-Edit, T-Spice W-Edit as a simulator. The supply voltage required for this VCO is 1.8V. In this VCRO firstly delay cell structure is developed and verified by Tanner EDA after that integrate the delay cell for ring VCO and sizing the device properly to achieve the desired output. Low power consumption is achieved by adjusting the supply voltage and input frequency also the low phase noise is achieved by proper sizing the transistor. The output of delay cell of VCO is shown in fig 5. Which contain the \( I_A, I_B & O_A, O_B \) as shown below.

The output of four stage ring VCO is shown in figure no.6 the performance comparisons of CMOS VCRO of various technologies are shown in Table 1.

<table>
<thead>
<tr>
<th>Sr. No</th>
<th>Architecture</th>
<th>Supply voltage (V)</th>
<th>Power (mW)</th>
<th>CMOS Process (µm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>4 stage, Dual delay loop [1]</td>
<td>3</td>
<td>-</td>
<td>0.6</td>
</tr>
<tr>
<td>2</td>
<td>2 stage, Single delay loop [2]</td>
<td>2.5</td>
<td>15.5</td>
<td>0.5</td>
</tr>
<tr>
<td>3</td>
<td>2 stage, Single delay loop [5]</td>
<td>1.8</td>
<td>65.5</td>
<td>0.18</td>
</tr>
<tr>
<td>4</td>
<td>4-stage, Dual delay loop [11]</td>
<td>1.8</td>
<td>13</td>
<td>0.18</td>
</tr>
<tr>
<td>5</td>
<td>3 stage, Single delay loop [14]</td>
<td>1.8</td>
<td>11.25</td>
<td>0.18</td>
</tr>
</tbody>
</table>
Compared to other research works, it is shown that the proposed VCRO consumes the lowest power, which is around 2.57 mW and phase noise is -110 dBc/Hz which is lower than other work.

V. CONCLUSION

The proposed Voltage controlled oscillator is fabricated in 0.18μm CMOS techniques. The centre frequency of VCO is 2.45GHz and operated at 1.8V supply voltage. In this VCO the four stage differential delay cell with single delay loop is used for development of VCO. The VCRO is designed by using the Tanner EDA V13 software. In this the low power consumption is achieved which is around 2.57mW and low phase noise which is -110dBc/Hz. This VCRO is efficient module for the Phase locked loop (PLL) because it consumes less power and phase noise is also low.

REFERENCES


AUTHOR BIOGRAPHY

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