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A Primary-Side Controlled Flyback LED Driver with Highly-Efficient Line Regulation

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***Abstract*—This paper presents a highly-efficient line regulation primary-side controlled flyback LED driver. Based on the current flyback topology, an 8-W prototype of the proposed flyback LED driver has been fabricated with a test chip. Experimental measurement results demonstrate that the proposed integrated implementation can efficiently enhance the line regulation less than 1%.**

***Index Terms*—LED driver, flyback converter, primary-side controlled, line regulation.**

LIST OF SYMBOLS

V_m	Peak amplitude of the AC input voltage.
ω_L	Angular frequency of the AC input voltage.
i_p	Current of the primary side.
i_{p_pk}	Sampled peak current of the primary side.
i'_{p_pk}	Physical peak current of the primary side.
i_{p_av}	Average current of the primary side.
i_s	Current of the secondary side.
i_{s_pk}	Peak current of the secondary side.
i_{s_av}	Average current of the secondary side.
V_{out}	Output voltage of the LED driver.
T_{on}	Duration time when the MOSFET switch is conductive.
T_{off}	Duration time when the MOSFET switch is cut-off.
T_{d_on}	Turn-on delay of the MOSFET switch.
T_{d_off}	Turn-off delay of the MOSFET switch.
T_{on_mos}	hysical conductive duration of the MOSFET switch.
L_m	Magnetizing inductance.

I. INTRODUCTION

ACCORDING to the statistical data of international energy agency (IEA), there has been 19 per cent global electric power consumed in illumination. In view of this, the traditional power-consumed incandescent lamps have recently been replaced with high power-efficient illumination. Furthermore, with the launch of the requirements of energy conservation and carbon reduction, LED illumination has become a promising alternative and an important approach for green source globally. An LED driver which can provide stable driving current for LED illumination is therefore highly desired [1]-[3]. In general, the design of LED driver circuits involves the considerations of small dimensions, long-life time, low cost, and high reliability [4]-[5]. Moreover, the evaluation factor of electricity efficiency, the power factor (PF) must be higher than 0.7 [6]. Therefore, an LED driver circuit design with high power factor (PF>0.95) is not only satisfying the requirement of solid state lighting (SSL), but also increasing power efficiency.

Conventionally, a constant-current LED driver for LEDs is realized using an isolated flyback converter with an output current regulation circuit as indicated in Fig. 1. Although this approach allows excellent LED current regulation, the output regulation circuitry requires an opto-coupler, reference voltage, and sense resistor, which increases system cost and deteriorates overall efficiency. By contrast, with the approach of the primary-side control, the opto-coupler will not be necessitated, which the cost can be further reduced and also the product dimension can be minimized. Furthermore, the present primary-side controlled flyback converters can achieve high power factor and perform current control, which are therefore widely employed in LED driver circuits [7]-[12].

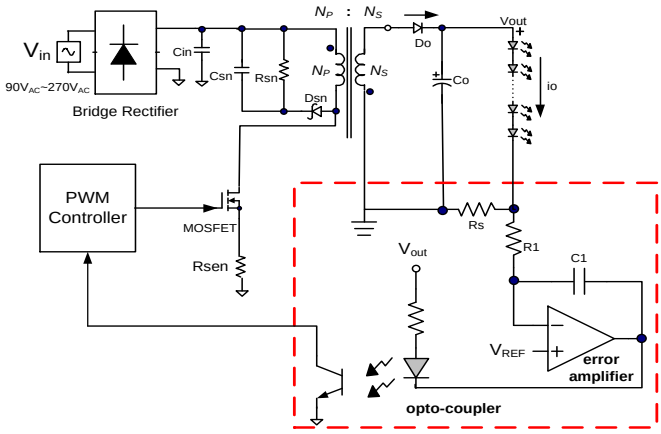

Fig. 1 Conventional isolated flyback converter for LED drivers.

Although primary-side controlled LED drivers are more attractive than isolated drivers in terms of lower fabrication cost and higher efficiency, the output current suffers the shortcomings of control delay phenomenon which deteriorates the characteristic of line regulation [13]-[19]. Several compensation schemes have been proposed [20]-[22]. An AC line compensation approach was proposed in [20], in which two compensation resistors were required to feed forward the input voltage and the sensed source voltage of the switching MOSFET. The output current regulation error was mainly due to the comparator delay T_d. Although the compensation approach could efficiently reduce the line regulation to near 1% with a fast comparator of T_d=200ns, the performance of line regulation could be worse simply due to the delay variation from the fluctuations of the supply voltage and temperature. A relatively simple compensation approach

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can be found in [21], in which a resistor and a capacitor were employed to form a delay network which provided an extra delay for compensation of source voltage of the switching MOSFET. Experimental results indicated the line regulation was 6.4% with an efficiency of 73.1%. In this paper, an integrated highly-efficient line regulation primary-side controlled flyback LED driver will be presented. To validate the performance of the proposed integrated LED driver, a prototype test chip is fabricated and the measurement results are provided.

II. THE SINGLE-STAGE PRIMARY-SIDE CONTROLLED FLYBACK DRIVER

The configuration and functional block diagram of the proposed controller for primary-side flyback LED driver circuits are shown in Fig. 2. The coil ratio n of the primary side to the secondary side is N_P / N_S.

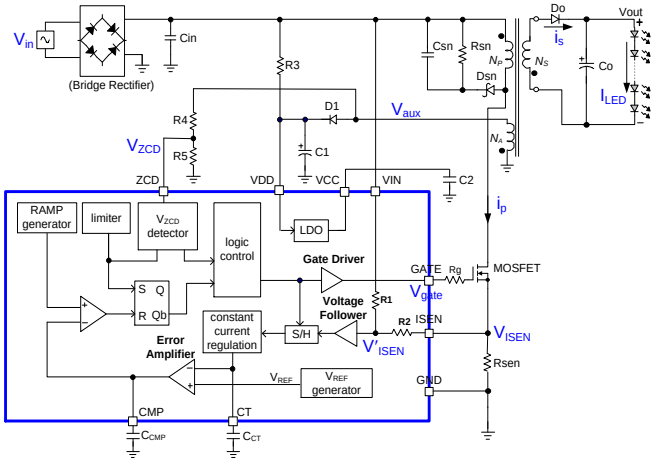

Fig. 2 Configuration of primary-side controlled flyback LED driver and the functional block diagram of the proposed controller with peak current compensation

Also note that the operation is under the conditions of the boundary conduction mode (BCM) and constant on-time control, in which the switching period of the MOSFET is T_s and we assume that the input signal is

$$V_{in}(t) = V_m \sin \omega_L t \tag{1}$$

Assuming the switching frequency fs of the MOSFET is much greater than the input voltage frequency fL, thus the input voltage can be regarded as a constant in a switching period. The input AC voltage can become a full-wave rectified DC voltage by using a bridge rectifier as shown in Fig. 2. In the first half cycle of the AC voltage, the LED current can be regarded as the average current which can be described as [19],

Clearly, the LED current is influenced by V_m and T_{on} as indicated in equation (2) when the parameters L_m, V_{out} and n are determined. Therefore, in order to maintain a constant LED current, the conductive time T_{on} has to be tunable for different V_m.

$$\begin{aligned} I_{LED} &= \frac{1}{\pi}\int_0^{\pi} i_{s\_av}(t)d\omega_L t = \frac{nV_m T_{on}}{2\pi L_m}\int_0^{\pi}\frac{T_{off}(t)}{T_s(t)}|\sin\omega_L t|d\omega_L t \\ &= \frac{nV_m T_{on}}{2\pi L_m}\int_0^{\pi}\frac{|\sin\omega_L t|^2}{|\sin\omega_L t| + \frac{V_{out}}{nV_m}}d\omega_L t \end{aligned} \tag{2}$$

III. PHENOMENON OF CONTROL DELAY

As indicated in equation (2), the conductive duration T_{on} of the MOSFET switch determines the LED current. The phenomenon of control delay, however occurs at the applications of physical circuit operation due to the parasitic capacitance at the gate of the MOSFET switch and the wire-loading capacitance of the printed circuit board. Moreover, the limitation of the driving capability of the MOSFET switch can further exacerbate the problem. These problems can result in the delays of the turn-on and turn-off operations of the MOSFET switch and influence the precision of the LED current control.

Due to the delay phenomenon, the V_{gate} voltage- controlled MOSFET switch will not response instantly. The phenomenon is especially serious when the MOSFET switch is from the status of conduction to cut off. The control delay will seriously lead to the inconsistence of the physical peak current $i'_{p\_pk}(t)$ and the sampled peak current $i_{p\_pk}(t)$ of the primary side as shown in Fig. 3.

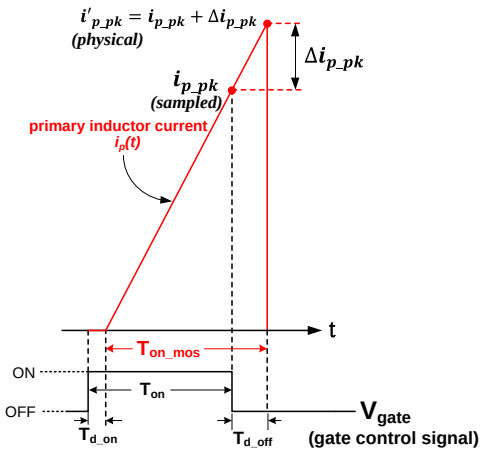

Fig. 3 Delay effect of gate control voltage on drain current of a MOSFET

Clearly, the MOSFET switch cannot turn on or turn off instantly when the gate voltage of the MOSFET V_{gate} is high as indicated in Fig. 3. The delay effect actually makes the sampled peak current i_{p_pk} deviated from the physical peak current i'_{p_pk} of the primary side, which influences the precision of the LED control current. The current difference can be represented with the following equation (3),

$$\begin{aligned} \Delta i_{p\_pk} &= i'_{p\_pk} - i_{p\_pk} \\ &= \frac{|V_{in}|}{L_m}\left(T_{on} - T_{d\_on} + T_{d\_off}\right) - \frac{|V_{in}|}{L_m}\left(T_{on} - T_{d\_on}\right) = \frac{|V_{in}|}{L_m}T_{d\_off} \end{aligned} \tag{3}$$

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in which the delay cut-off time T_{d_off} is determined by the selected values of off-chipped components, the parasitic capacitances of the MOSFET and the PCB routing effect. The physical output LED current can also be described as,

$$I'_{LED} = \frac{n}{2\pi}\int_0^{\pi}\frac{T_{off}(t)}{T_s(t)}\cdot i'_{p\_pk}(t)d\omega_L t = I_{LED} + \frac{nV_m T_{d\_off}}{2\pi L_m}\int_0^{\pi}\frac{T_{off}(t)}{T_s(t)}\cdot|\sin\omega_L t|d\omega_L t \quad (4)$$

and the current difference of the output LED current can therefore be represented as,

$$\Delta I_{LED} = I'_{LED} - I_{LED} = \frac{nV_m T_{d\_off}}{2\pi L_m}\int_0^{\pi}\frac{T_{off}(t)}{T_s(t)}\cdot|\sin\omega_L t|d\omega_L t \quad (5)$$

Obviously, the peak current difference Δi_{p_pk} and the output LED current difference ΔI_{LED} are dependent upon the input voltage amplitude V_m, which it can deteriorate the line regulation of the system.

IV. THE PEAK CURRENT COMPENSATION TECHNIQUE

From the previous observation we know that the drain current of the MOSFET switch increases linearly at the cut-off period T_{d_off} whereas unfortunately, the source voltage V_{ISEN} of the MOSFET does not increase linearly at the period for physical circuit operation as shown in Fig. 4(b).

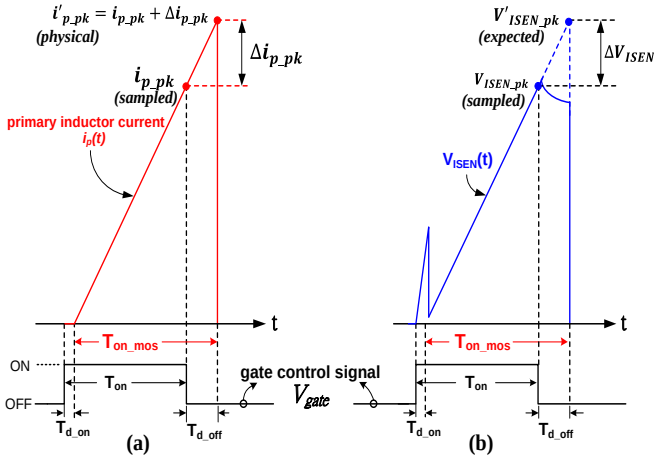

Fig. 4 Relationship of gate control voltage and drain current under the delay effect of gate control voltage (a) MOSFET drain current (b) MOSFET source voltage V_{ISEN}

The voltage difference of the expected source peak voltage and the sampled source peak voltage of the MOSFET is given by

$$\Delta V_{ISEN} = V'_{ISEN\_pk} - V_{ISEN\_pk} = \frac{|V_{in}|}{L_m}R_{sen}(T_{on} - T_{d\_on} + T_{d\_off}) - \frac{|V_{in}|}{L_m}R_{sen}(T_{on} - T_{d\_on}) = \frac{T_{d\_off}R_{sen}}{L_m}|V_{in}| \quad (6)$$

The difference is mainly due to the parasitic capacitor sharing part of the drain current of the MOSFET since at the period T_{d_off} the MOSFET drain current cannot flow through the resistor R_{sen} to ground completely, part of the current still flows through the parasitic capacitor C_{gs} as indicated in Fig. 5. Therefore, it is difficult to obtain the physical peak current i'_{p_pk} just by detecting the source voltage in physical circuits.

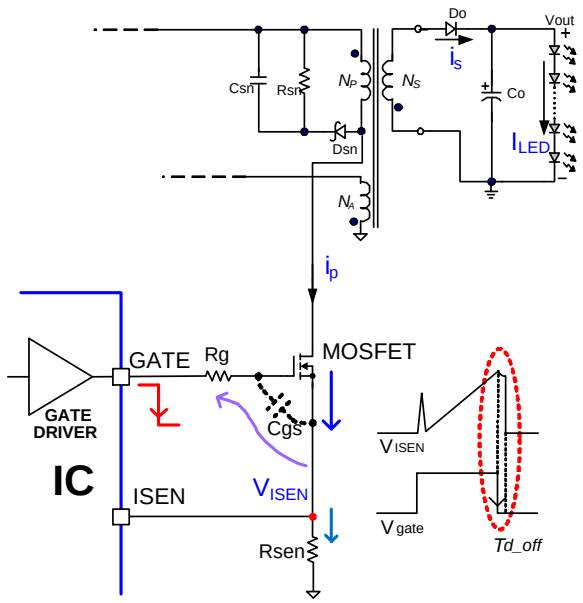

Fig. 5 Relationship of delay cut-off time (*Td_off*) and the parasitic capacitor (Cgs) of the MOSFET switch

Since the sampled peak voltage is V_{ISEN_pk} which is not the expected peak voltage V'_{ISEN_pk} and also the expected peak voltage cannot be obtained in physical circuit operation, a compensation approach is proposed in this paper, which the expected peak voltage V'_{ISEN_pk} can be obtained under the effect of cut-off delay operation as shown in Fig. 6. The compensation can be realized with the employment of resistors R1 and R2 as illustrated in Fig. 2, in which we assume that the resistance R_{sen} is much less than the resistances of R1 and R2. By employing superposition theorem and note that $|V_{in}| >> V_{ISEN}$, the voltage V'_{ISEN} can be obtained approximately as indicated in equation (7)

$$V'_{ISEN}(t) = \frac{R2}{R1+R2}\left(|V_{in}| - V_{ISEN}\right) + V_{ISEN} \approx \frac{R2}{R1+R2}|V_{in}| + V_{ISEN} = \Delta V_{ISEN} + V_{ISEN} \quad (7)$$

By substituting ΔV_{ISEN} indicated in equation (6) into equation (7), we can obtain equation (8). When the inductance L_m, resistance R_{sen} and other component values are determined, the value of T_{d_off} is also determined. Therefore, the effect of cut-off delay can be compensated by properly selecting the resistances R1 and R2.

$$\Delta V_{ISEN} = \frac{R2}{R1+R2}|V_{in}| = \frac{T_{d\_off}R_{sen}}{L_m}|V_{in}| \quad (8)$$

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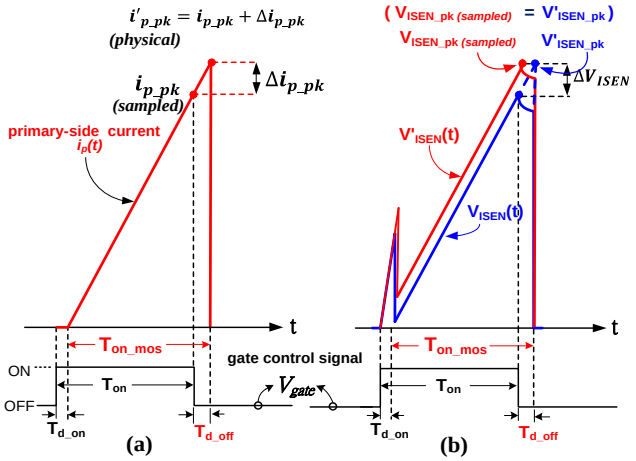


Fig. 6 Schematic of peak current compensation mechanism (a) MOSFET drain current (b) MOSFET source voltage V_{ISEN}

V. CIRCUIT REALIZATION

The realized architecture of the proposed primary-side controlled flyback LED controller IC shown in Fig. 2 mainly comprises the circuit blocks of, (*A*) Peak-current sampling circuit (*B*) Output driving stage (*C*) Zero cross detector (*D*) Ramp waveform generator. The peak-current compensated amount is related to the delay time and in general, the delay time is approximately 200ns~600ns which is dependent upon the component values and PCB Layout. Detailed description of the operation will be addressed in the following several sub-sections.

A. Peak-Current Sampling Circuit

The realization of the peak-current sampling circuit is shown in Fig. 7(a), in which the voltage V_{ISEN} is converted into current with a voltage-to-current converter. Moreover, the circuit of transistor MP2 cascaded with transistor MP1 together with amplifier OPA1 is employed to reduce the current deviation due to the effect of channel modulation of transistor MP1. In other words, amplifier OPA1 makes the drain voltage of transistor MP1 follow the gate voltage V_{mp1} and the output voltage of OPA1 also provides the gate bias for transistor MP2. With the cascaded configuration, transistor MP1 can provide precise peak current i_{p_pk}. The transmission-gate switch *S1* and resistor R1 are employed to prevent transistor MP1 from the transient disturbance of the switch *S2*.

B. Output Driving Stage

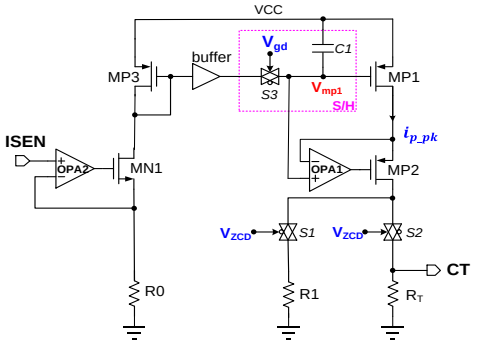
The function of the output driving stage is to drive the off-chipped power MOSFET. In the proposed flyback LED driver, two voltage supplies are employed: one is VDD (high voltage) which is for off-chipped power MOSFET and the other is on-chipped voltage supply VCC (low voltage) which is generated with low dropout regulator (LDO). The stage comprises two level-shifters and an output MOS driver as shown in Fig. 7(b). The input signal CLK is a PWM signal whose level is from 0 to VCC. With the employment of the output driving stage, the signal level increases to VDD which can drive the external power MOSFET.

C. Zero Cross Detector (ZCD)

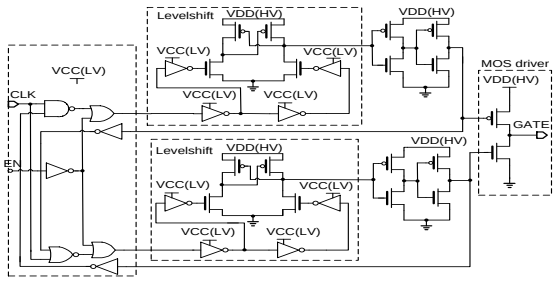
The ZCD shown in Fig. 7(c) is employed to detect the output voltage of the secondary-side coil. By detecting the voltage of VZCD, the ZCD can detect the time which starts to release power and the time which the operation has completed. When the flowing current decreases to zero, the output signals of ZCD can trigger the next operation.

D. Ramp waveform generator

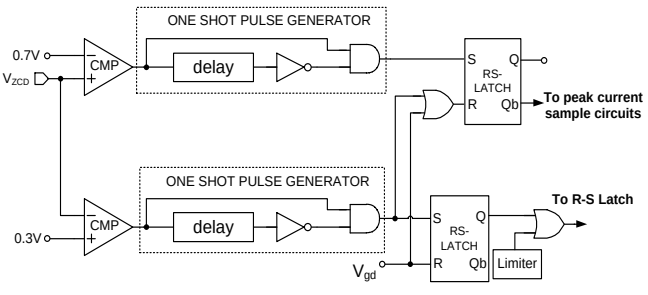
The conductive duration of the MOSFET switch shown in Fig. 2 is determined by the voltages of VCMP and VRAMP. The operation of the ramp waveform generator shown in Fig. 7(d) can be described as: when the MOSFET shown in the RAMP generator is conductive, the voltage VRAMP increases linearly until it reaches to VCMP. The output of CMP comparator is in high level, which resets the RS-LATCH and in turn cuts off the off-chipped MOSFET switch. Therefore, the conductive time of the off-chipped MOSFET switch is proportional to the voltage VCMP.



(a)



(b)



(c)

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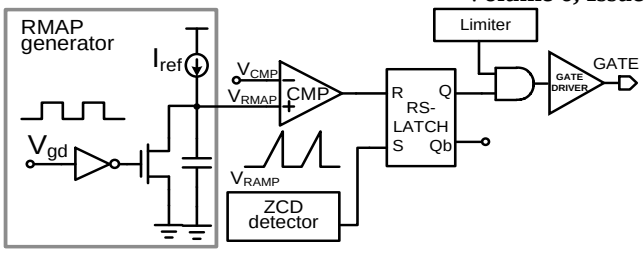

(d)

Fig. 7 (a) Block diagram of the peak current sampling circuit (b) Schematic of the output driving stage (c) Schematic of the zero cross detector (d) Schematic of the ramp waveform generator

VI. EXPERIMENTAL AND MEASURED RESULTS

The test chip for the verification of the proposed primary-side controlled flyback LED driver with highly-efficient line regulation has been implemented with TSMC 0.25µm CMOS High-Voltage Mixed-Signal process technology. The micro-photograph of the realized test chip is shown in Fig. 8, which the die size including bonding pads is 1.200×1.280 mm2.

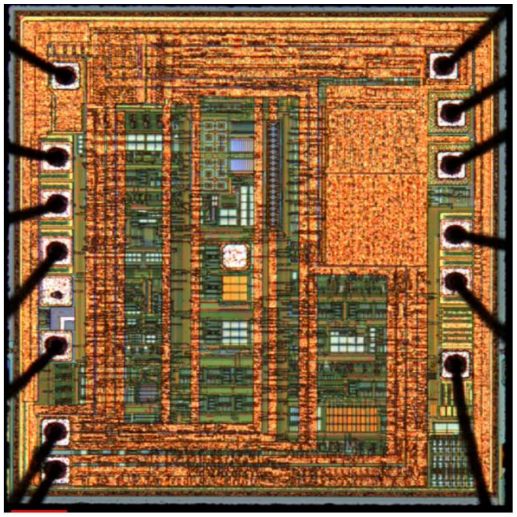

Fig. 8 Microphotograph of the test chip

Fig. 9 shows the measured RMS currents for the input voltages of 110V_{AC}, which the measured current is 387mA.

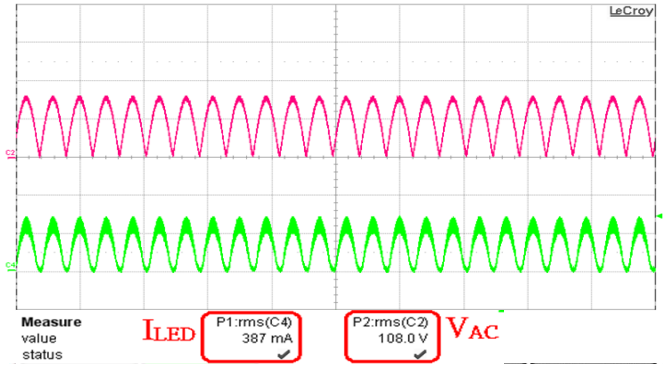

Fig. 9 LED current waveforms (upper waveform: output voltage waveform of bridge regulator, lower waveform: I_{LED} current waveform)

The measured LED currents for different AC input voltages are shown in Fig. 10. Clearly, the proposed LED driver can achieve the line regulation of the LED driver efficiently, which the line regulation is approximately 0.91%.

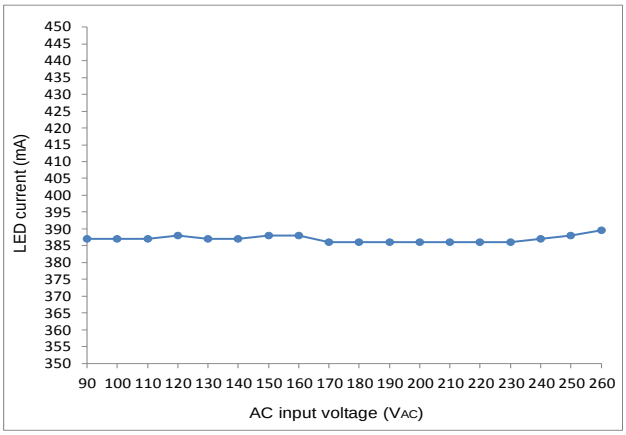

Fig. 10 Measured LED current versus AC input voltage (V_{AC})

The measured power efficiencies for different AC input voltages of the proposed LED driver are shown in Fig. 11, which indicate the efficiency is higher for a lower input voltage. This can be explained with the switching loss since the switching frequency is lower for a lower input voltage and the switching loss is also lower. Fig. 11 also indicates the maximum efficiency is approximately 91% for the input voltage of 150V_{AC} and the efficiency can always remain above 89.2% for universal line operation.

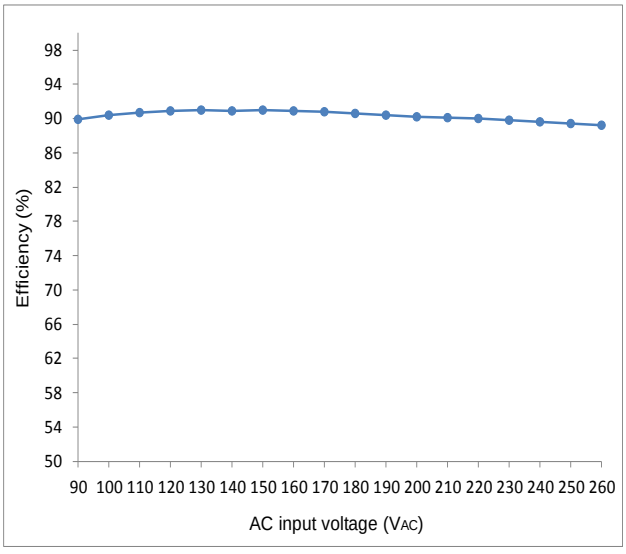

Fig. 11 Measured power efficiency versus AC input voltage (V_{AC})

The measured power factors for different input voltages are shown in Fig. 12, which indicate the power factors are all over 96%. Table I shows the performance of the proposed LED driver. Comparisons with other published works are also indicated in Table II. Obviously, the proposed LED driver has a higher efficiency, a better line regulation with high output power compared with other selected previous works.

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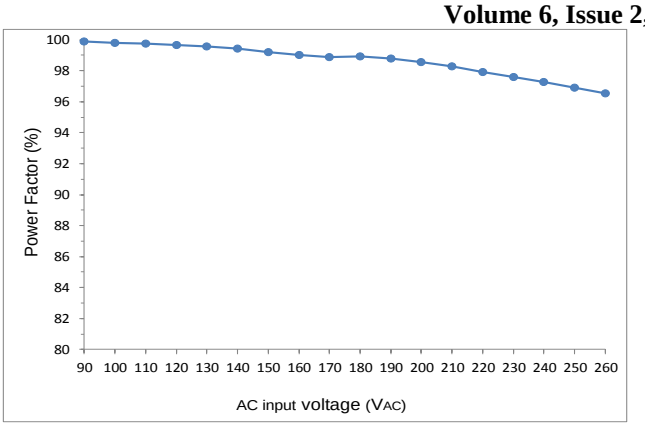

Fig. 12 Measured power factor versus AC input voltage (V_{AC})

TABLE I: PERFORMANCE SUMMARY

Technology	TSMC 0.25μm
Chip Size (with PADs)	1.20×1.28 mm^2
AC input voltage	90-260V_{AC} (RMS)
output current	0.387A
Maximum switching frequency	100 kHz
Maximum efficiency	91 %
Power factor	> 96 %
Line regulation	< 1 %

TABLE II: PERFORMANCE COMPARISONS WITH OTHER PUBLISHED WORKS

	This Work	[20]	[21]	[22]
Technology	Integrated (TSMC 0.25 μm)	Discrete	Discrete	Integrated (TSMC 0.35 μm)
Chip size (with pads)	1.2×1.28 mm^2	n/a	n/a	1.2×1.5 mm^2
AC input voltage	90-260 V_{AC}	90-265V_{AC}	60-260 V_{AC}	85-264 V_{AC}
Maximum switching frequency	100 kHz	67 kHz	130 kHz	60 kHz
Maximum efficiency	91%	85.5%	73.1%	84%
Power factor	>96%	92~99%	n/a	n/a
Line regulation	< 1%	1%	6.4%	±1%
Output power	8W	8.5W	3W	3W

VII. CONCLUSION

In this paper, we have proposed a constant-current LED driver and its operation. The feasibility has been verified with the experimental measured results, which the line regulation is less than 1%. Moreover, the proposed approach is compatible with the existed LED control technology and easy to implement. Therefore, it is very suited for universal line LED illumination.

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