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Design rules of the CMOS inverter for voltage converters

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Abstract*—This paper presents a description of the dominantcharacteristics of the CMOS inverter, which is used for voltage converters–charge pumps applications. This circuit controls transport charge between main capacitors to create a higher DC voltage. The significant part of the pump losses is caused by the inverter cross current. This current flows through the inverter in transition state and discharges the capacitor, therefore decreases the pump voltage gain. The CMOS inverter design is based on the analog block description for high-voltage integrated circuits using BSIM model equations. The main benefit of this article is derivated analytical relationship between width and length of the NMOS and PMOS transistors to achieve the static power minimization. The derivation has been performed based on the sensitivity analysis. The design relationship are applicable to the other MOSFET models, as EKV. The characteristic of the proposed circuit has been verified by simulation in ELDO Spice. Analysis results show that the cross current is reduced by ten times in comparison with the value of the standard digital inverter (with symmetrical voltage transfer characteristics). This improvement was achieved while keeping relatively large area of both transistors satisfying the dynamic properties.

***Index Terms*—CMOS inverter, cross current, charge pump,BSIM model, high-voltage, sensitivity.**

I. INTRODUCTION

A CMOS inverter is a basic block (Fig. 1) for digitaldesign circuits which performs a logic operation from A to A.However, there are also aplications in the analog domain; bothcontinuous–time circuits (oscillators, amplifiers) and discrete–time analog circuits (voltage convertors). Although discrete–timeanalog circuits seem to be digital circuits from a system perspective, the internal state of the system is time continuousduring each period of the clock signal. Charge pumps ([6], [7],[8]) are a typical group of switched–capacitor (SC) circuits,where the inverter drives switch to a transport charge betweenthe main capacitors. The output voltage of the inverter with acapacitive load may be in an undefined state from the view oflogic levels because *energy* accumulated in capacitors *must be a continuous function oftime*. Results of the transientanalysis show that the dominant part of losses in chargepumps is caused by a DC cross current that flows throughan inverter operating in the linear region of voltage transfercharacteristics. This is undesirable *because the cross current greatly decreases a pump´s voltage gain* while losses causedby propagation delays of the inverter are very small.

Current research deals with the dynamic behavior of theinvertor and transistor sizing, which is based on the *equivalent digital model*. A number of detailed analyses in digital circuits([1], [4], [12]–[19]) have been reported ([15]–[19]). The inverteroperating in a strong inversion is known. The width of thePMOS must be 2-3 times width of the NMOS [1] (symmetricaltransfer characteristics). However, this setting may not suit inanalog circuits.

In the article, the inverter design for voltage converters is discussed in order to minimize the average cross current duringthe period of the clock signal. Using BSIM model equations,an analytical description of DC characteristics ([1], [4]) willbe found for this purpose. The strong inversion region isexpected in the high-voltage circuits, where the behavior ofthe MOSFET models for analog structured design is correct. Consequently, it is not necessary to admit a specified technology,because the EKV parameters are extracted from thecurves simulated using the BSIM models [3]. The main benefitof this article is an *analytical relationship* between sizing(width and length) of both the transistors to achieve the staticpower minimization of the charge pump inverter. The acquiredestimation can be used as the baseline for the optimizingalgorithm.

II. BSIM MODEL EQUATION

A real model of the MOSFET, like BSIM involves manyeffects [2]. It contains many model parameters and any derivation is very difficult (implicit form, solving of irrational equations, etc.). So, the equations are simplified to only describe the dominant characteristics for the design purpose. The static model of MOSFET is discussed as introduced in the previous text.

For MOSFET operation in high-voltage circuits where $V_{GS} \ll V_{TH}$, the following conditions must be true:

- long channel MOSFET
- strong inversion region.

Channel length is an important parameter because of the breakdown voltage. The electrical field in a structure induced by an applied voltage must be significantly less than the critical electrical field, $E = \frac{V}{L_{eff}} \leq E_{crit}$, where L_{eff} is effectivechannel length. A critical electrical field is limited to the valuegiven by a semi-empiric model [2].

The effective channel length is relative to the applied voltage *Vmax* (gate-source, drain-source) defined as

$$L_{eff} \gg V_{max} \frac{\mu_{eff}}{2v_{sat}}, \qquad (1)$$

where $v_{sat}$is the saturation velocity (model parameter) and $\mu_{eff}$is effective mobility.

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A drain current model is given by a single equation [2]. The transition from triode to the saturation region is ensured through an effective drain-source voltage.

$$V_{DSeff} = \begin{cases} V_{DS}, & \text{for triode region} \\ V_{DSsat}, & \text{for saturation region} \end{cases} \quad (2)$$

and for long channel MOSFETs, the saturation drain current $V_{DS} = V_{DSsat}$is given by:

$$(3) \quad I_{Dsat0} = \frac{1}{2}\frac{W}{L} c_{oxe} \mu_{eff} V_{DSsat}(V_{GS} - V_{TH}),$$

where $c_{oxe}$is the electrical oxide capacitance. The boundary between the triode and saturation regions is predicted by the voltage (V_{GS}- V_{TH}) and applies a bias voltage effect and further model parameters (channel length and width...) included in the bulk-charge equation [2], labeled A_{bulk}. A_{bulk} is closed to unity for relatively high source-bulk bias voltage. In the other words,

$$V_{DSsat} = \frac{V_{GS} - V_{TH}}{A_{bulk}} \approx V_{GS} - V_{TH} \text{ for } V_{SB} > V_{GS}. \quad (4)$$

Generally, the output I-V curve in the saturation region(V_{DS}> V_{DSsat}) is written by several physical mechanisms.Nevertheless, considering the condition (1) short channel effect- channel length modulation (CLM) and Substrate CurrentInduced Body Effect (SCBE) can be neglected. Then the draincurrent increases linearly with the V_{DS} voltage. The slope ofthe output characteristics is mainly determined by Early voltageV_{ADIBL} due to the drain-induced barrier lowering (DIBL)effect ([1], [2], [5]). V_{ADIBL} is directly proportional to thevoltage V_{GS}, as is shown bellow. Moreover, the equation (5)contains the model parameters PDIBLC2 and PDIBLCB [2].

$$V_{ADIBL} = \frac{1}{2}\frac{V_{GS} - V_{TH}}{\text{PDIBLC2}\,(1 - \text{PDIBLCB}\,V_{SB})} \quad (5)$$

The complex drain current equation may be expressed by the formula

$$I_{Dsat} = I_{Dsat0}\left(1 + \frac{V_{DS} - V_{DSsat}}{V_{ADIBL}}\right)$$

for $V_{DS} \geq V_{DSsat}$.

The drain current in the triode region is a function of theV_{DS} voltage (V_{GS} = const.). The maximum of the parabolicfunction I_{DS0} =f(V_{DS}) corresponds to the voltage V_{DSsat}because of the neglected CLM mechanism ([1], [2], [5]). Then,the relationship between the drain-source voltage V_{DS} and thesaturation drain current I_{Dsat0} [5] can be written simply as

$$I_{DS0}(V_{DS}) = -\frac{I_{Dsat0}}{V_{DSsat}^2} V_{DS}^2 + \frac{I_{Dsat0}}{V_{DSsat}} 2V_{DS}$$

for $V_{DS} < V_{DSsat}$.

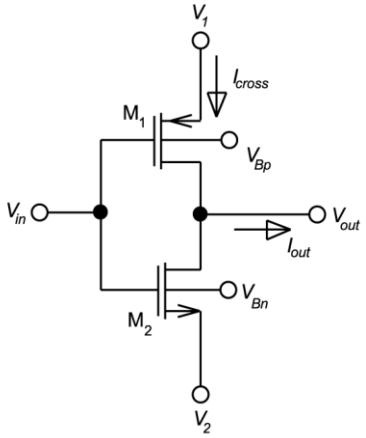

Fig. 1. The CMOS inverter.

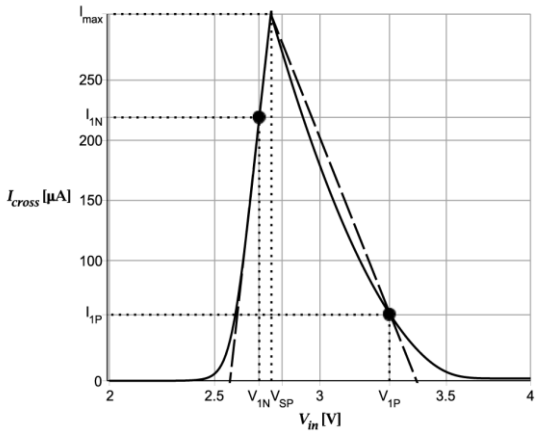

Fig. 2. DC current characteristics of the inverter.

III. STATIC PARAMETERS OF THE CMOS INVERTER

A diagram of the CMOS inverter schematic is shown in Fig. 1. All voltages are referenced to the *ground* and $V_1 - V_2 > V_{THN} + |V_{THP}|$.

The inverter´s cross current characteristics is shown in Fig. 2. A general form of the analytical expression of the cross current is divided into the three cases:

$$I_{cross} = \begin{cases} I_{DsatN}|V_{GS} = V_{in} - V_2, & \text{for C1} \\ I_{DsatP}|V_{SG} = V_1 - V_{in}, & \text{for C2} \\ 0, & \text{otherwise,} \end{cases} \quad (8)$$

where condition C1 is: $V_2 + V_{THN} \leq V_{in} \leq V_{SP}$and C2 is: $V_{SP} \leq V_{in} \leq V_1 - |V_{THP}|$.

Cross current is maximal at the switching point V_{in} = V_{SP},see [1]. Both transistors M_1 and M_2 are in the saturationregion (Eq. 6) for this case and the drain current of eachMOSFET must be equal:

$$I_{DsatN}|_{V_{GS}=V_{SP}-V_2} = I_{DsatP}|_{V_{SG}=V_1-V_{SP}}, \quad (9)$$

if the output current (see Fig. 1) is zero (I_{out} = 0). Equation(9) is more than third order for variable V_{SP}, thus simplifyingpreconditions will be introduced.

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Firstly, Early voltage (Eq. 5) limits to infinity, wherefromit is compared $I_{Dsat0N} \approx I_{Dsat0P}$. Secondly, the absolutelyvalue of the drain currents of the PMOS and NMOStransistors for the derivation V_{SP} are not important; onlytransconductance is important. The slope of the cross currentcharacteristics on each interval is mainly given by the linearpart of the voltage V_{GS}- $V_{TH}(V_{SB})$(MOS transconductancein strong inversion is a linear function of the gate-sourcevoltage), while other powers at that voltage are not taken intoaccount. Hence, the bulk charge equation [2] is adjusted to

$$A_{bulk0}(V_{SB}) = A_{bulk}|_{(V_{GS}-V_{TH})_{eff}=0}$$

and with the effective mobility substituted into the equation(3) at zero bias voltages. Finally, the formula of the switchingpoint for the BSIM model [1] can be expressed in the modifiedform:

$$V_{SP} = \frac{V_1 - |V_{THP}(V_{BS})| + \sqrt{R\frac{a}{b}}[V_2 + V_{THN}(V_{SB})]}{1 + \sqrt{R\frac{a}{b}}}, \quad (10)$$

where $a = \frac{c_{oxeN}\mu_{effN}|_{V_{GS}=V_{SB}=0}}{A_{bulk0N}|_{V_{SB}=0}}$, $b = \frac{c_{oxeP}\mu_{effP}|_{V_{SG}=V_{BS}=0}}{A_{bulk0P}|_{V_{BS}=0}}$ and $R = \frac{W_n}{L_n}\frac{L_p}{W_p}$.

The switching point is an important parameter for the calculation of DC power because of the discontinuous cross current characteristics at that point, as it is shown in Fig. 2. The typical characteristics of the dependence of the switching point on the ratio dimensions of bothtransistors is shown inFig. 3.

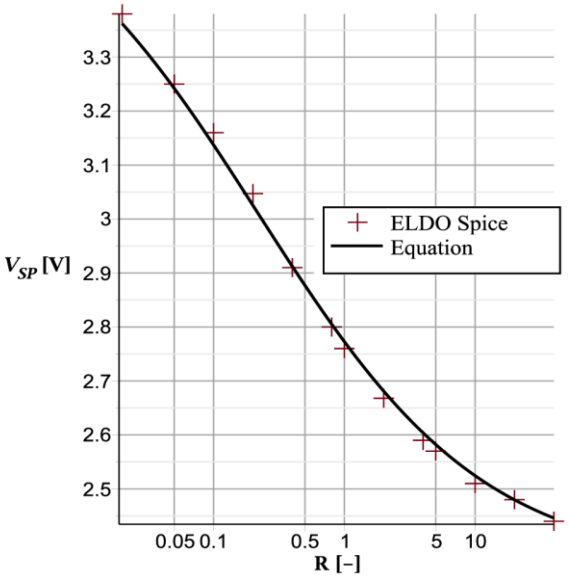

Fig. 3. Switching point analysis – dependence on the ratio *R*

Static power during the inverter´s output voltage crossingbetween logic 1 and logic 0 is defined as

$$P_{DC} = \int_{V_2}^{V_1} I_{cross}(V_{in})\, dV_{in} = \int_{V_2+V_{THN}}^{V_{SP}} I_{DsatN}(V_{in})\, dV_{in} + \int_{V_{SP}}^{V_1-|V_{THP}|} I_{DsatP}(V_{in})\, dV_{in}. \quad (11)$$

The solution of equation (11) exists, but it is confusing and unnecessary for the estimation of the power dissipation.Results of the numeric integration of equation (11) shows thatfunction is primarily determinend by the function arctan[1],that *can be approximated by its argument (linear function) at zero*$\lim_{x\to 0}\left(\frac{\arctan(x)}{x}\right) = 0$. A simpler approach is based onan approximation of the characteristics (Fig. 1) in intervals $V_{in} \in \langle V_2 + V_{THN}, V_{SP}\rangle$ and $V_{in} \in \langle V_{SP}, V_1 + |V_{THP}|\rangle$by*linear interpolation* for two points at each interval:

- At the point coressponding to the known voltage V_{SP}that is substituted into equation (5):

$$I_{max}|_{V_{in}=V_{SP}} = I_{DsatN}|_{V_{GS}=V_{SP}-V_2} \simeq \simeq I_{DsatP}|_{V_{SG}=V_1-V_{SP}}$$

At the point where $|V_{GS}|$ is greater than the thresholdvoltage $|V_{TH}|$ (strong inversion region), the transistoris operating at the edge of the saturation region(M_1 for $V_{in} \in \langle V_{SP}, V_1 + |V_{THP}|\rangle$ and $M_2$for $V_{in} \in \langle V_2 + V_{THN}, V_{SP}\rangle$), where the drain current is approximatelythe linear function of the gate-source voltage. Itmeans that quadratic part of V_{GS} voltage from expression$(V_{GS}\text{-}V_{TH})^2$ must be less than its linear part. Assumingthe equality of these parts, two solutions exists. Thefirst one is $V_{GS} = 0$ that is ignored and the secondis $V_{GS} = 2|V_{TH}|$[2]:

$$I_1 = \begin{cases} I_{1N} = I_{Dsat0N}|_{V_{GS}=V_{1N}=2V_{THN}}, & \text{for NMOS} \\ I_{1P} = I_{Dsat0P}|_{V_{SG}=V_{1P}=2|V_{THP}|}, & \text{for PMOS} \end{cases}$$

thence, new formula for cross current characteristics can be expressed as

$$\tilde{I}_{cross} \approx \begin{cases} I_{1N}\frac{V_{SP}-V_{in}}{V_{SP}-V_2-2V_{THN}} + I_{max}\frac{V_2+2V_{THN}-V_{in}}{V_2+2V_{THN}-V_{SP}}, & \text{for C1} \\ I_{1P}\frac{V_{SP}-V_{in}}{V_{SP}-V_1+2|V_{THP}|} + I_{max}\frac{V_1-2|V_{THP}|-V_{in}}{V_1-2|V_{THP}|-V_{SP}}, & \text{for C2} \\ 0, & \text{otherwise,} \end{cases} \quad (12)$$

where condition C1 is: $V_2 + V_{THN} \leq V_{in} \leq V_{SP}$ and C2is: $V_{SP} < V_{in} \leq V_1 - |V_{THP}|$. The equation (12) allows tocalculate the static power as the triangle area:

$$\tilde{P}_{DC} \approx \frac{1}{2} I_{max}\left(\frac{I_{max}(V_1 - 2|V_{THP}|) - I_{1P}V_{SP}}{I_{max} - I_{1P}} - \frac{I_{max}(V_2 + 2V_{THN}) - I_{1N}V_{SP}}{I_{max} - I_{1N}}\right). \quad (13)$$

[1]Analytical expression is given by the sum of the functions *arctan* and *ln*.
[2]This value is also included in the coefficient at the *arctan* in the solutionof Eq. (11).

The average current during the transition between both the logiclevels is the coinciding DC power divided by the power supplyvoltage:

$$I_{av} = \frac{P_{DC}}{V_1 - V_2}. \quad (14)$$

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IV. STATIC POWER MINIMIZATION

Static power dissipation dependence on the dimensions ofboth transistors M_1 and M_2 is discussed in this section. Staticpower is reduced by reducing an inverter´s peak current (Fig.2) I_{max} = f(V_{SP}). Implying that, the switching point shouldbe closed to voltage V_2+V_{THN}(lower limit) or V_1-|V_{THP}|(upper limit) to turn off one of either transistor (equation 13).However, this state cannot really be obtained because $R\rightarrow$ 0for the lower limit or $R\rightarrow\infty$ for the upper limit (Fig. 3),as it is shown in Fig. 3. The setting of the optimal ratio $R$to effective reduction of static power can be found by thesenstivity analysis of the switching point to the parameter R(Eq. 10). The sensitivity is defined as

$$C = \frac{\mathrm{d}V_{SP}}{\mathrm{d}R}\frac{R}{V_{SP}} = -\frac{1}{2}\frac{a\,R\,(V_1 - |V_{THP}| - V_2 - V_{THN})}{\left(\sqrt{\frac{a}{b}R}+1\right)\sqrt{\frac{a}{b}R}\,b}\cdot \cdot\frac{1}{\sqrt{\frac{a}{b}R}\,(V_2+V_{THN})+V_1-|V_{THP}|} \quad (15)$$

and decrease of the maximum sensitivity to the desired valueis expressed by parameter δ:

$$\delta = \frac{C_{opt}}{C_{max}}. \quad (16)$$

The δ parameter will be determined by the simulations results as it is shown bellow. *δ is usually put to 0.5*because the voltageV_{SP} depends on the square root of R. Maximum sensitivity(in absolute value) given by the condition $\frac{dC}{dR} = 0$ is at thepoint

$$R_{Cmax}|_{C=C_{max}} = \frac{V_1 - |V_{THP}|}{\frac{a}{b}(V_2+V_{THN})}. \quad (17)$$

The normalized sensitivity curve to the maximum absolute value is shown in Fig. 4.

Finally, the optimal parameter R is derived from equations(15), (16) and (17),

$$R_{opt} = \frac{1}{16}\left[\frac{2C_{max}\delta\,(V_{1a}+V_{2a})+V_{12}}{\sqrt{\frac{a}{b}}C_{max}\delta V_{2a}} \pm \right. \pm \left.\frac{\sqrt{V_{12}}\sqrt{4C_{max}\delta\,(V_{1a}+V_{2a}+C_{max}V_{12}\delta)+V_{12}}}{\sqrt{\frac{a}{b}}C_{max}\delta V_{2a}}\right]^2, \quad (18)$$

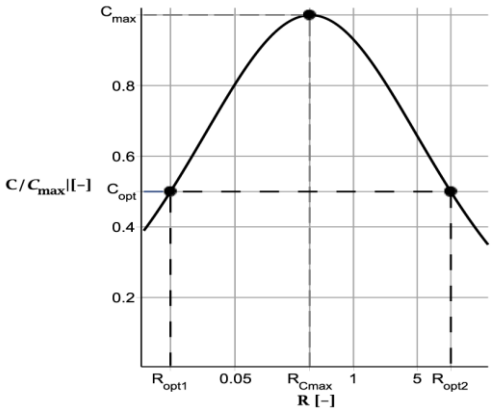

Fig. 4. Normalized sensitivity curve

where V_{1a} = V_1- |V_{THP}|, V_{2a} = V_2 + V_{THN} and V_{12} = V_{1a}-V_{2a}. Two solutions for the equation (18) exists. The first:$R_{opt1}$for $\frac{W_n}{L_n} \gg \frac{W_p}{L_p}$and the second: R_{opt2} for $\frac{W_p}{L_p} \gg \frac{W_n}{L_n}$(Fig. 3). The calculated ratio R dependence on the chosenparameterδ is shown in Tab. II.

V. SIMULATION RESULTS

The DC parameters of the CMOS inverter were simulatedby ELDO. The simulation circuit parameters are shown inTab. I. The dependence of the average cross current (Eq. 14)on the width of the PMOS (W_p) or NMOS (W_n) transistorwas analyzed at the fixed channel lengths L_n, L_p. These weredetermined based on the condition (1), respecting the value ofthe bis voltages, as it is shown in Table I.

TABLE I: SIMULATION CIRCUIT PARAMETERS

	Parameter	Value
Power supply voltages	V_1	4 V
	V_2	2 V
Threshold voltage of the N/PMOS	V_{THN}	0.356 V
	$\|V_{THP}\|$	0.33 V
Coefficients calculated from Eq.10	a	$3.43\cdot10^{-4}$ AV^{-2}
	b	$7.45\cdot10^{-5}$ AV^{-2}

Analysis results in Tab. II show that an effective reduction ofI_{av} is achieved when $R \gg R_{Cmax}$ (solution R_{opt1} of Eq. 18),consequently $W_n \gg W_p$ and V_{SP} approach the lower limit,$V_{SP}\rightarrow V_2 + V_{THN}$. This is physically caused by a greatermobility of electrons in the NMOS structure compared to themobility of holes in the NMOS dimensions. Otherwise, when$R \ll R_{Cmax}$, a very large disproportion between sizes of bothtransistors adversaly affects other properties of the inverter(transistors area, dynamic properties,...), as is shown bellow. Of course, the mean value of the cross current is not only a function of R, but depends on the specific value ofW_n/L_n, W_p/L_p respectively, as is shown in Fig. 5. Thespecific sizes of the NMOS and PMOS transistors can be setby additional application requirements (time delay, switchingcharacteristics), but the ratio R must be retained. *Experience says that the optimal value of the parameter δ* is 0:4 ÷ 0:6*(Eq. 16) for practical design*. Values of the ratio R and theaverage cross current I_{av} for this range of the δ parameter arebold in Tab. II.

TABLE II: SIMULATION RESULTS

Channel length of the N/PMOS: $L_p = L_n = 1\mu m$				
Width of the N/PMOS:			$W_n = 40\,\mu$m	$W_p = 40\,\mu$m
δ	$\mathbf{R_{opt1,2}}$[-]	$\mathbf{V_{SP}}$ [V]	$\mathbf{I_{av}}$ [mA]	
0.51	**0.01**	3.47	1.92	**0.018**
0.63	**0.02**	3.4	1.69	**0.031**
0.92	0.1	3.16	1.07	0.106
0.985	0.2	3.047	0.798	0.159
1	0.34	2.76	0.309	0.309
0.83	2	2.67	0.186	0.372
0.7	4	2.59	0.107	0.430
0.66	**5**	2.57	**0.089**	0.447
0.5	**11.7**	2.5	**0.047**	0.507
0.41	**20**	2.46	**0.026**	0.541
0.31	40	2.42	0.013	0.582

However, the optimal setting of R may not be optimal for the design of an inverter operating in digital circuits, where

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the switching point (Eq. 10) should be closed to the ideal valueof half of the supply voltage. Therefore

$$R|_{V_{SP}=V_{DD}/2} = \frac{b}{a}\left[\frac{V_1 - V_2 - 2\,|V_{THP}(V_{BS})|}{V_1 - V_2 - 2V_{THN}(V_{SB})}\right]^2 \quad (19)$$

and corresponding sensitivity is about 0.98 and simulated I_{av}value is about ten times higher compared to the optimizationprocess. The width of the PMOS transistor is sized to 2 ÷ 3the width of the PMOS [1] transistor (lengths are the same),provided that $V_{THN} \approx |V_{THP}|$. This condition can not besatisfied in voltage convertors due to a different supply voltageV_1, V_2in each of the convertor´s stages and the differentthreshold voltage of each of the transistors (body effect, [1]–[5]).

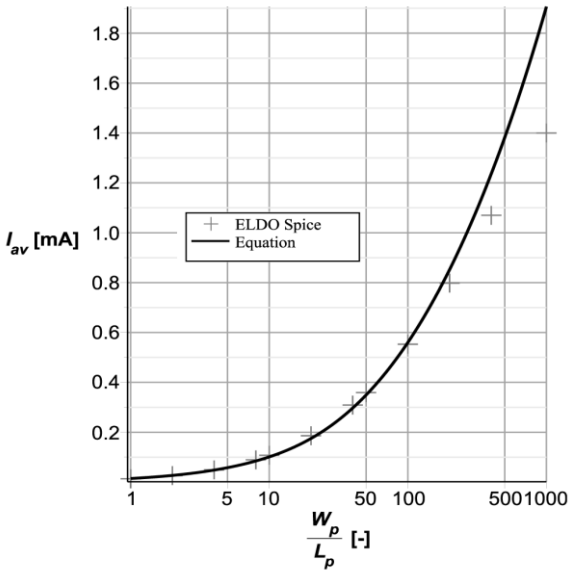

Fig. 5. Cross current vs. the W_p/L_p ratio

VI. CONCLUSION

The inverter draft for charge pump applications as an analogblock is discussed in this paper. Design process via *the symbolic description* is based on the low cross current (Eq. 8)during the transition between logic high and logic low levels.The sensitivity analysis of the switching point to the sizingof the transistors (Fig. 4) shows that it is possible to find theoptimal ratio$R=\frac{W_n}{L_n}\frac{L_p}{W_p}$, while keeping a relatively big ratioW/L value of each of the NMOS and PMOS transistors. It isvery favorable from a time response perspective. The formulaederived in this paper are applicable to the other MOSFETmodels including the parameters for the specified technologyprocess. Important implications of the optimization processcan be summarized in the following items:

- Asymmetric DC characteristics; switching point is notequal to the half supply voltage. It is not an appropriateconfiguration in a digital circuit (rise time versus fall time,noise margine for high versus low logic level,...), whilethese properties are not meaningful in analog ciruits. Thisfact has not been solved yet.
- Propagation delays between logic levels should be shortbecause of the possibility of setting small effectiveswitching resistances (large width) of the NMOS andPMOS. Propagation delays are not the same.
- The cross current is very small if the operating pointof the inverter is set to the linear region of the voltagetransfer characteristics in comparison with cross currentof the ”symetrical” inverter of the same area.
- Static and dynamic properties are insensitive to the dimensionaltolerance of the transistors. The sensitivity ofthe proposed inverter switching point to the transistorssizing is always less than sensitivity of the inverter fordigital circuit applications. It follows from the principleof the design process.

All proposals were validated by the real circuit simulations.

Charge pumps are systems that are usually designed via thesimulation because of its properties taken from both digitaland analog circuits (Discrete-time analog circuits). Testing andmany iterations mean long-time simulation process. Thus, the analytical results will be very useful for the prediction of the required static and dynamic properties of these circuits (output voltage, rise time, etc.) without optimization process.

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