A Hybrid PWM Controller IC for DC-DC Buck Conversion with Table Look-Up PID Compensator

Steve Hung-Lung Tu, Hsin-Wei Yeh

Abstract—a novel PWM single-chip controller IC with table look-up PID compensator for output voltage regulation is presented, which can achieve a minimum embedded memory requirement. The controller employs analog hysteresis voltage comparators, a 4-level error process unit (4-level EPU), a memory-reused PID compensator and a low-power-consumption digital PWM. Based on the efficient memory-access mechanism, the controller can alleviate the penalty of large amount of embedded memory employed for table look-up based PID compensation. The proposed controller has been validated with test-chip measurement results which demonstrate feasibility of the proposed approach.

Index Terms—PWM, PID compensator, buck conversion.

I. INTRODUCTION

DC-DC buck conversion increasingly becomes a highly desired built-in function in power management circuits and systems [1]–[3]. Among these power regulation approaches, digital power regulation controllers play an important role due to their inherently low sensitivity to environmental interference and the progress of the digital technologies. Analog-to-digital (A/D) converters have been also employed in controllers as the interface due to the inherently analog regulated output voltage [4]-[5], where an n-bit A/D converter were employed to increase the conversion speed. However, due to the high-complexity of the conventional A/D converter and the non-linearity of the delay-line A/D converter, the function of the A/D conversion was performed with an analog comparator and an EPU [6], which the state transition of the EPU state machine was triggered with the feedback error signal to regulate the system output voltage. Moreover, a fully table look-up approach for the controller was proposed in [5], in which the operation results of the PID compensator and the PWM were pre-calculated and stored in an external memory. The input data to the compensator is acted as the address to access the memory and the memory output can develop a 1-MHz clock signal with tunable duty cycle. Due to the employment of a memory for the main part of the controller, the structure of the proposed controller is regular, which is suitable for VLSI implementation and also avoids performing complicated calculation. According to the report in [5], however the memory usage can be further enhanced for the direct implementation of the approach. In this paper, we investigate an efficient memory-access mechanism to further enhance the memory requirement for the table look-up based PID compensation together with test chip experimental measurement results.

II. THE PROPOSED CONTROLLER ARCHITECTURE

Fig. 1 shows the proposed controller IC for power regulation, which comprises two analog comparators with / without hysteresis characteristic, a 4-level EPU, a table look-up based PID compensator and a digital PWM. \( V_{\text{ref}} \) is the reference voltage employed to compare with the regulated output voltage \( v_{\text{out}}(t) \) and yields a 2-bit error signal with four possible binary values \( 2'b00 / 2'b01 / 2'b10 / 2'b11 \) from the comparators. With the 4-level EPU, the four possible binary values can develop an error signal \( e(n) \) ranging from \(-4 \) to \( +4 \) to represent the output regulated voltage with tuning range from \(-V_{\text{max}}/2 \) to \(+V_{\text{max}}/2 \) [4]. The PID compensator and the digital PWM generate output signal \( \text{duty}(t) \) which is a signal of 1-MHz frequency with tunable duty cycle. According to \( \text{duty}(t) \) and all internal parameters, the converter develops the regulated output voltage \( v_{\text{out}}(t) \) with an off-chip switching buck converter and the operation of the controller iterates until \( v_{\text{out}}(t) \) is equal to \( V_{\text{ref}} \).

![Fig. 1 Block diagram of the proposed controller for power regulation](image-url)

One of the comparators employed in the proposed controller has the characteristic of hysteresis, in which the hysteresis width is set at 0.01V and the reference voltage \( V_{\text{ref}} \) is set at 1.8V. Therefore, the regulated voltage \( V_{\text{out}} \) has a \( \pm 0.005V \) transition voltage.
A. 4-Level Error Process Unit (EPU)

Fig. 2 depicts the four levels, A, B, C, D developed from the comparison of \( v_{out}(t) \) and \( V_{ref} \). The relationships and the coding of the signal error are shown in Table I, in which \( V_q \) is defined as the resolution of the output regulated voltage, which is equal to \((\Delta v_{out})_{max}/8\) [4].

\[
e(n) = e(n-1) + a \cdot e(n) + b \cdot e(n-1) + c \cdot e(n-2)
\]

B. PID Compensator and Digital PWM

For a table look-up based configuration, the most general control law performs the following discrete-time PID control law [7],

\[d(n) = d(n - 1) + a \cdot e(n) + b \cdot e(n - 1) + c \cdot e(n - 2)\]  \hspace{1cm} (1)

Fig. 2 Generation of the 4 levels from the comparators

The 4-level EPU operation diagram is shown in Fig. 3(a), which its operation can be described as follows. Assuming an iterative signal \( v_{out}(t) \) is required to trace the reference signal \( V_{ref} \) and let \( \text{error} \) be the output of the comparators, which is coded according to Table I.

\[
e(n) = \begin{cases} 10 & \text{error} = 11 \\ 1 & \text{error} = 10 \\ 01 & \text{error} = 01 \\ 00 & \text{error} = 00 \end{cases}
\]

Fig. 3 (a) Operation diagram of the 4-level EPU (b) State relationships with the two compared voltages

As the controller starts to operate, the 4-level EPU state machine starts to work depending on the 2-bit input signal \( \text{error} \) from the comparators. If the input signal is 11 and \( e(n) \) is not equal to +4, then \( e(n) = e(n - 1) + 1 \), else if the input signal is 00 and \( e(n) \) is not equal to -4, \( e(n) = e(n - 1) - 1 \), otherwise \( e(n) = e(n - 1) \). Obviously, it can be implemented with a 4-bit register to cover the range from -4 to +4 as shown in Fig. 3(b). \( e(n) \) is thus the output of the 4-level EPU, which indicates the present state of the 4-level EPU state machine and it is also proportional to the difference of \( V_{ref} \) and \( v_{out}(t) \).

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The parameters of the PID compensator are, $a = 25$, $b = -47$, $c = 23$, which the calculation of these parameters can be referred to [6] and the sum of equation (1) can be calculated with the Euler’s method [8]. Note that the sum can be pre-calculated and stored the values in the embedded memories. The experimental test chip is designed and fabricated with TSMC 0.35-μm mixed-signal double-poly-four-metal (2P4M) polyide CMOS technology. Fig. 6 shows the chip microphotograph, which the chip area is 1478μm × 1438μm including the bonding pads and the active region is only 723μm × 719μm.

The measured result of power-up transient period is shown in the upper waveform of Fig. 7. Obviously the convergent time is approximately 95μs.

Fig. 7 Measured waveform of $v_{out}(t)$ at the power-up transient

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III. EXPERIMENTAL RESULTS

The proposed controller has been validated with test chip measurement results for the condition of, the line voltage $V_g = 3.3V$, the output voltage is regulated at $V_{out} = 1.8V$, the load resistor $R_{load} = 3.6Ω$, $L = 47μH$, $C = 100μF$, in which $L$ and $C$ are employed in the off-chip switching buck converter.

![Fig. 4 Block diagram of the multiple-access PID compensator and digital PWM](image)

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![Fig. 5 Operation timing of a simplified 4-bit digital PWM](image)

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output voltages are stable for both transient responses. Performance characteristics of the implemented controller IC are summarized in Table II.

4-level EPU state machine, table look-up based PID compensator, and digital PWM have been implemented with hardware description language (HDL) and embedded memories, which only occupied approximately 0.5 mm² of silicon area in a standard 0.35μm CMOS process.

REFERENCES


