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A Hybrid PWM Controller IC for DC-DC Buck Conversion with Table Look-Up PID Compensator

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Abstract*—a novel PWM single-chip controller IC with table look-up PID compensator for output voltage regulation is presented, which can achieve a minimum embedded memory requirement. The controller employs analog hysteresis voltage comparators, a 4-level error process unit (4-level EPU), a memory-reused PID compensator and a low-power-consumption digital PWM. Based on the efficient memory-access mechanism, the controller can alleviate the penalty of large amount of embedded memory employed for table look-up based PID compensation. The proposed controller has been validated with test-chip measurement results which demonstrate feasibility of the proposed approach.

***Index Terms*—PWM, PID compensator, buck conversion.**

I. INTRODUCTION

DC-DC buck conversion increasingly becomes a highly desired built-in function in power management circuits and systems [1]–[3]. Among these power regulation approaches, digital power regulation controllers play an important role due to their inherently low sensitivity to environmental interference and the progress of the digital technologies. Analog-to-digital (A/D) converters have been also employed in controllers as the interface due to the inherently analog regulated output voltage [4]-[5], where an n-bit A/D converter were employed to increase the conversion speed. However, due to the high-complexity of the conventional A/D converter and the non-linearity of the delay-line A/D converter, the function of the A/D conversion was performed with an analog comparator and an EPU [6], which the state transition of the EPU state machine was triggered with the feedback error signal to regulate the system output voltage. Moreover, a fully table look-up approach for the controller was proposed in [5], in which the operation results of the PID compensator and the PWM were pre-calculated and stored in an external memory. The input data to the compensator is acted as the address to access the memory and the memory output can develop a 1-MHz clock signal with tunable duty cycle. Due to the employment of a memory for the main part of the controller, the structure of the proposed controller is regular, which is suitable for VLSI implementation and also avoids performing complicated calculation. According to the report in [5], however the memory usage can be further enhanced for the direct implementation of the approach. In this paper, we investigate an efficient memory-access mechanism to further enhance the memory requirement for the table look-up based PID compensation together with test chip experimental measurement results.

II. THE PROPOSED CONTROLLER ARCHITECTURE

Fig. 1 shows the proposed controller IC for power regulation, which comprises two analog comparators with / without hysteresis characteristic, a 4-level EPU, a table look-up based PID compensator and a digital PWM. V_{ref} is the reference voltage employed to compare with the regulated output voltage $v_{out}(t)$ and yields a 2-bit *error* signal with four possible binary values 2'b00 / 2'b01 / 2'b10 / 2'b11 from the comparators. With the 4-level EPU, the four possible binary values can develop an error signal *e(n)* ranging from –4 to +4 to represent the output regulated voltage with tuning range from $-(\Delta v_{out})_{max}/2$ to $+(\Delta v_{out})_{max}/2$ [4]. The PID compensator and the digital PWM generate output signal *duty(t)* which is a signal of 1-MHz frequency with tunable duty cycle. According to *duty(t)* and all internal parameters, the converter develops the regulated output voltage $v_{out}(t)$ with an off-chip switching buck converter and the operation of the controller iterates until $v_{out}(t)$ is equal to V_{ref}.

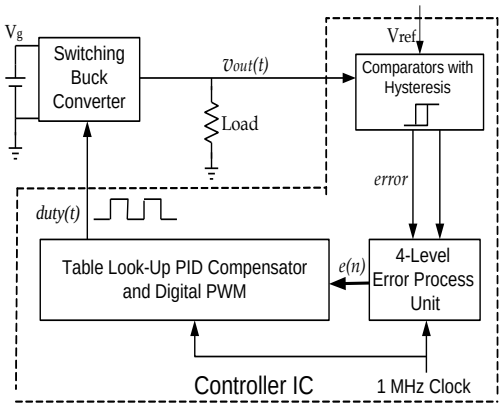

Fig.1 Block diagram of the proposed controller for power regulation

One of the comparators employed in the proposed controller has the characteristic of hysteresis, in which the hysteresis width is set at 0.01V and the reference voltage Vref is set at 1.8V. Therefore, the regulated voltage Vout has a ±0.005V transition voltage.

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A. 4-Level Error Process Unit (EPU)

Fig. 2 depicts the four levels, A, B, C, D developed from the comparison of $v_{out}(t)$ and V_{ref}. The relationships and the coding of the signal error are shown in Table I, in which V_q is defined as the resolution of the output regulated voltage, which is equal to $(\Delta v_{out})_{max}/8$ [4].

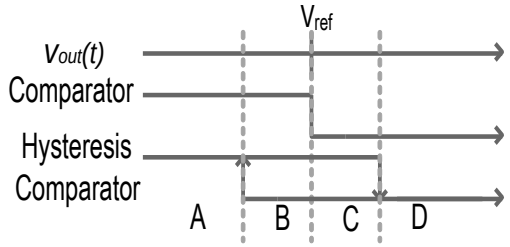

Fig.2 Generation of the 4 levels from the comparators

TABLE I. Signal Coding for the Four Levels

	A	B	C	D
	$Vref-vout(t) \geq Vq$	$0 \leqq Vref-vout(t) < Vq$	$-Vq \leqq Vref-vout(t) < 0$	$Vref-vout(t) < -Vq$
error	11	10	01	00

The 4-level EPU operation diagram is shown in Fig. 3(a), which its operation can be described as follows. Assuming an iterative signal $v_{out}(t)$ is required to trace the reference signal V_{ref} and let *error* be the output of the comparators, which is coded according to Table I.

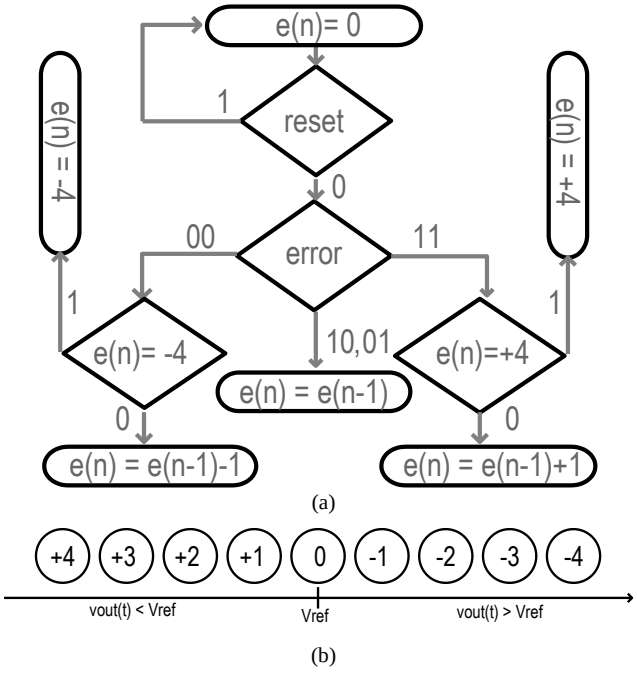

Fig.3 (a) Operation diagram of the 4-level EPU (b) State relationships with the two compared voltages

As the controller starts to operate, the 4-level EPU state machine starts to work depending on the 2-bit input signal *error* from the comparators. If the input signal is 11 and *e(n)* is not equal to +4, then *e(n)=e(n-1)+1*, else if the input signal is 00 and *e(n)* is not equal to -4, *e(n)=e(n-1)-1*, otherwise *e(n)=e(n-1)*. Obviously, it can be implemented with a 4-bit register to cover the range from –4 to +4 as shown in Fig. 3(b). *e(n)* is thus the output of the 4-level EPU, which indicates the present state of the 4-level EPU state machine and it is also proportional to the difference of V_{ref} and $v_{out}(t)$.

B. PID Compensator and Digital PWM

For a table look-up based configuration, the most general control law performs the following discrete-time PID control law [7],

$$d(n) = d(n-1) + a\cdot e(n) + b\cdot e(n-1) + c\cdot e(n-2) \quad (1)$$

Which indicates that the new compensated value, *d(n)*, can be computed with the past compensated value, *d(n-1)*, and the present and past values of the error signals, *e(n)*, *e(n-1)*, and *e(n-2)*. Since *a*, *b*, *c* are constants, the products $(a\cdot e)$, $(b\cdot e)$ and $(c\cdot e)$ can be implemented with look-up tables *a*, *b*, and *c*, respectively. Note that in addition to memories for the look-up tables, we also require three 8-bit adders to compute equation (1). An alternative approach is being the employment of a larger memory to achieve "fully table look-up" [5], in which a $2^{17}\times 8$ memory is required to implement the table directly and even requires $2^{20}\times 8$ embedded memory if 4-bit *e*(*n*), *e*(*n-1*), *e*(*n-2*) and 8-bit *d*(*n-1*) are employed for an SOC design. To gain more insight, however the correlation between the three consecutive iteration error signals *e*(*n*), *e*(*n-1*), and *e*(*n-2*) of the 4-level EPU state machine makes the 12-bit address only have 71 possibilities, which greatly reduces the memory requirement. In this paper, the memory access approach takes advantages of the correlation of the three error signals for the table look-up computation. Hence,

$$d'(n) \equiv f_1\left[a\cdot e(n) + b\cdot e(n-1) + c\cdot e(n-2)\right] \quad (2)$$

Note that the 71 possible permutations only lead to less than 16 possible $d'(n)$, which can be coded with 4-bit data. The 4-bit $d'(n)$ can be obtained with a simple logic circuit, which is used as the 4-bit LSBs together with the 8-bit *d*(*n-1*) as the 8-bit MSBs to combine as the 12-bit address to retrieve memory and obtain *d*(*n*). Therefore,

$$d(n) = f_2\left[d(n-1), d'(n)\right] \quad (3)$$

The block diagram of the memory-access PID compensator is indicated in the right part of Fig. 4. Note that in the proposed controller, the compensated signal *d(n)* is ranging from 1 to 254. The digital PWM employed in this paper is based on a ring-oscillator/counter approach as shown in the left part of Fig. 4. The high-resolution, high-frequency digital PWM can be achieved by employing hybrid embedded ring-oscillator and counter approach. For a 1-MHz system clock, an equivalent 256-MHz operating frequency can be obtained by employing an embedded 16-bit ring-oscillator to generate q(15:0) and a 4-bit counter to provide cnt(15:0). The embedded ring-oscillator can be implemented with D-type

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flip-flops as shown in the sub-figure of the left part of Fig. 4.

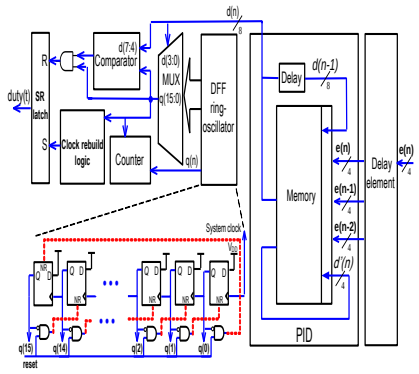

Fig. 4 Block diagram of the multiple-access PID compensator and digital PWM

Fig. 5 shows the operation timing of a simplified 4-bit digital PWM. The embedded ring oscillator generates q(3:0) with overlapped clock signals. At the beginning of a switching cycle, the output SR latch is set, and the digital PWM output signal duty (t) goes high. The output signal of the ring oscillator q(3:0) serves as the clock for the counter. The complete switching period is divided into $2^2 \times 2^2 = 16$ time slots. The counter performs the first two MSBs of the digital input d(n) (*i.e.* the duty ratio command), and the ring-oscillator outputs q(3:0) carry out the remnant LSBs of d(n). When the combined output word from the counter and ring-oscillator matches the digital input d(n), the output flip-flop is reset and the output pulse goes low. In the example waveforms of Fig. 5, the duty ratio of the output pulse is 11/16. Note that all the transition edges of the signals indicated in the 4-bit example shown in Fig.5 are lined-up with an equivalent 16MHz clock edges.

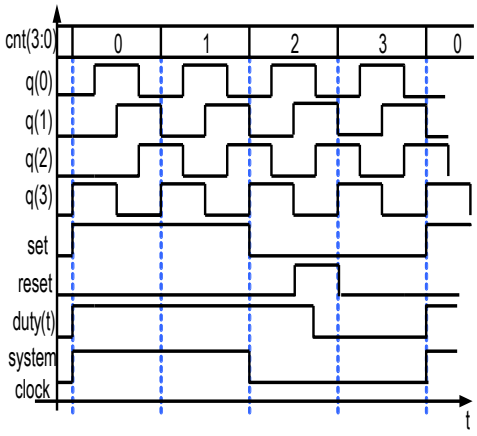

Fig. 5 Operation timing of a simplified 4-bit digital PWM

III. EXPERIMENTAL RESULTS

The proposed controller has been validated with test chip measurement results for the condition of, the line voltage V_g = 3.3V, the output voltage is regulated at V_{out} = 1.8V, the load resistor R_{load} = 3.6Ω, L = 47μH, C = 100μF, in which L and C are employed in the off-chip switching buck converter. Moreover, the parameters of the PID compensator are, a = 25, b = –47, c = 23, which the calculation of these parameters can be referred to [6] and the sum of equation (1) can be calculated with the Euler's method [8]. Note that the sum can be pre-calculated and stored the values in the embedded memories. The experimental test chip is designed and fabricated with TSMC 0.35-μm mixed-signal double-poly-four-metal (2P4M) polycide CMOS technology. Fig. 6 shows the chip microphotograph, which the chip area is 1478μm × 1438μm including the bonding pads and the active region is only 723μm × 719μm.

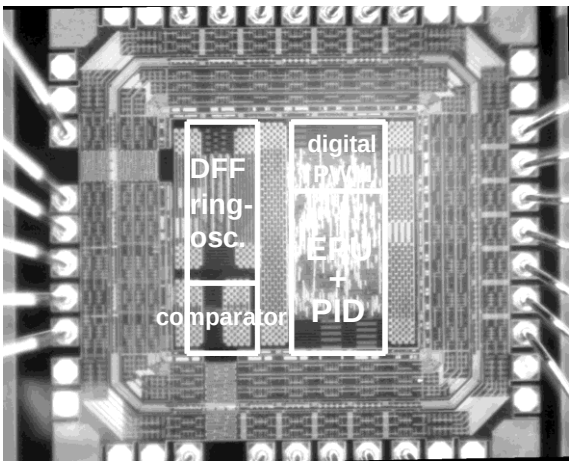

Fig. 6 Chip microphotograph of the proposed PWM controller IC

The measured result of power-up transient period is shown in the upper waveform of Fig. 7. Obviously the convergent time is approximately 95μs.

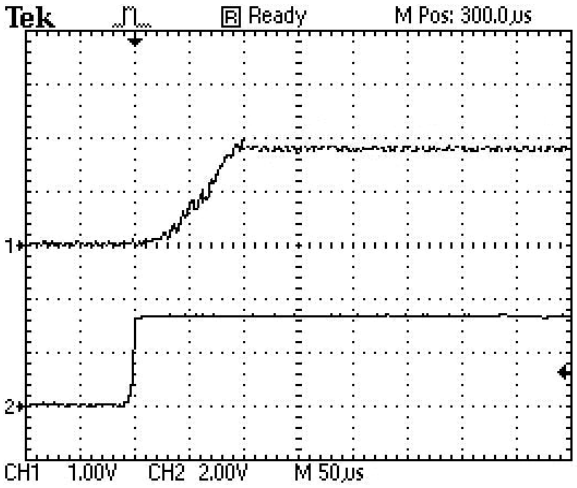

Fig. 7 Measured waveform of $v_{out}(t)$ at the power-up transient

Fig. 8 shows the load transient response from 500mA to 100mA (the output load is from 3.6Ω to 18Ω). The upper waveform is the regulated output voltage $v_{out}(t)$ and the lower waveform is the load current. Fig. 9 indicates the line transient response for the case of line voltage V_g from 4.2V to 3.3V. The upper waveform is the regulated output voltage and the lower waveform is the line voltage. Clearly, the regulated

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output voltages are stable for both transient responses. Performance characteristics of the implemented controller IC are summarized in Table II.

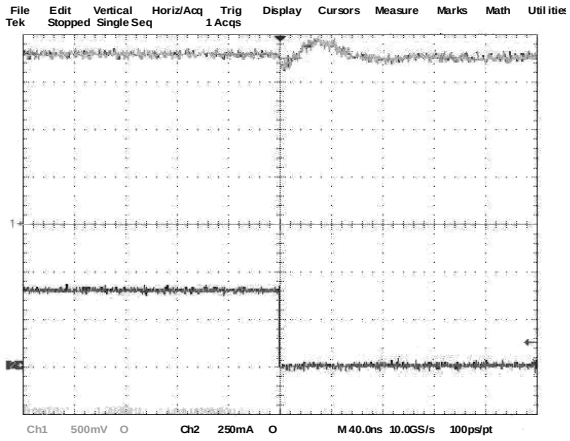

Fig. 8 Waveforms for load transient response

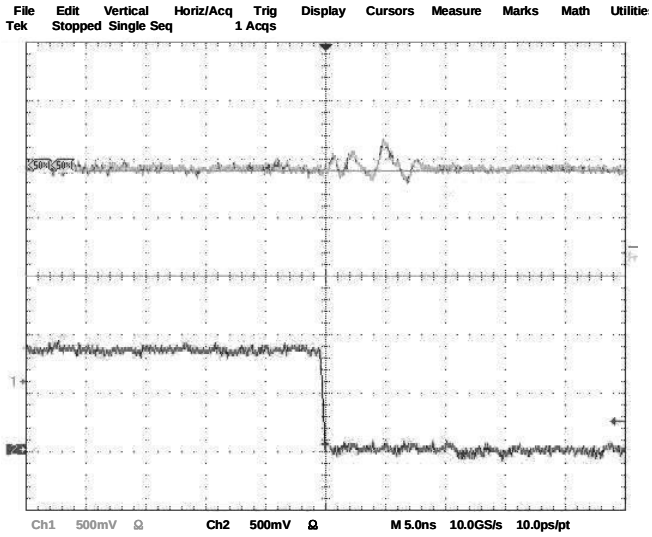

Fig. 9 Waveforms for line transient response (V_g is from 4.2V to 3.3V)

TABLE II. PERFORMANCE SUMMARY OF THE CONTROLLER IC

Technology	TSMC 0.35μm, 2-poly, 4-metal CMOS
Line input voltage	3.3V
Regulated output voltage	1.8V
Power-up transient time	95μs
Switching frequency	1MHz
Steady-state vout ripple	60mV
Power efficiency	96%
Active die size	0.715×0.706mm^2

IV. CONCLUSION

A novel PWM controller IC based on the proposed table look-up mechanism for DC-DC buck conversion has been presented together with test chip experimental measurement results. The employment of comparators with hysteresis can stabilize the 4-level EPU state transition. Furthermore, the 4-level EPU state machine, table look-up based PID compensator, and digital PWM have been implemented with hardware description language (HDL) and embedded memories, which only occupied approximately 0.5 mm^2 of silicon area in a standard 0.35μm CMOS process.

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