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Modelling of Cuk Rectifier for Power Factor Correction

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Abstract*— Cuk converter is a dc-dc converter; it can use for step up and step down of voltage by varying duty ratio. cuk converter have low ripples in output. cuk converter can use for power factor correction applications by operating discontinuous mode, there switching occurs in zero values of current .discontinuous means current approaches to zero, when supply voltage and current are in phase ,power factor changes to unity. if load is capacitive, output voltage have to buck still supply voltage and current are In phase, that is unity power factor.

***Index Terms*— Bridgeless rectifier, Cuk converter, power factor correction (PFC), Discontinuous conduction mode (DCM).**

I. INTRODUCTION

Power supplies with active power factor correction (PFC) techniques are becoming necessary for many types of electronic equipment to meet harmonic regulations and standards. Most of the PFC rectifiers utilize a boost converter at their front end. Efficiency of conventional PFC scheme was less due to significant losses in the diode bridge. Significant conduction loss, caused by the forward voltage drop across the bridge diode, considerably reduces the converter's efficiency, especially at a low line input voltage. In order to maximize the power supply efficiency, research efforts are directed towards designing of bridgeless PFC circuits, where losses due to large number of semiconductors is reduced by essentially eliminating the full bridge input diode rectifier. A bridgeless PFC rectifier allows the current to flow through a minimum number of switching devices compared to the conventional PFC rectifier. Accordingly, the converter conduction losses can be significantly reduced and higher efficiency can be obtained, as well as cost savings. Recently, several bridgeless PFC rectifiers have been introduced to improve the rectifier power density and/or reduce noise emissions via soft-switching techniques or coupled magnetic topologies. A bridgeless buck PFC rectifier was proposed in for many step-down applications. But, the input line current cannot follow the input voltage around the zero crossings of the input line voltage; besides, the output to input voltage ratio is limited to half. Also, buck PFC converter results in an increased total harmonic distortion.

II. PROPOSED BRIDGELESS CUK PFC RECTIFIERS

Cuk converter is a dc-dc converter; it can step up and step down the voltage according to the variation in duty ratio,

$$\frac{Vo}{V} = \frac{D}{1-D}.$$

The analysis assumes that the converter is operating at a steady state in addition to the following assumptions: pure sinusoidal input voltage, ideal lossless components, and all capacitors are large enough such that their switching voltage ripples are negligible during the switching period *Ts* .Moreover, the output filter capacitor *Co* (*Co* 1 and *Co* 2 for topology 2) has a large capacitance such that the voltage across it is constant over the entire line period. During the positive half cycle of line voltage, the first dc–dc Cuk circuit, L_1–Q_1–C_1–$L_{o\,1}$–$D_{o\,1}$, is active through diode D_p which connects the input ac source to the output. During the negative half cycle of line voltage, the second dc–dc Cuk circuit, L_2–Q_2 -C_2–$L_{o\,2}$–$D_{o\,2}$, is active through diode D_n , which connects the input ac source to the output. The average voltage across capacitor C_1 during the line cycle can be expressed as follows:

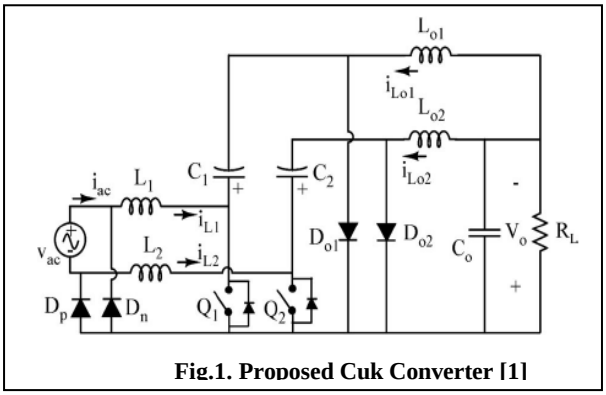

Fig.1. Proposed Cuk Converter [1]

$$v_{C_1}(t) = \begin{cases} v_{ac}(t) + V_o, & 0 \le t \le \dfrac{T}{2} \\ V_o, & \dfrac{T}{2} \le t \le T \end{cases}$$

Due to the symmetry of the circuit, analysis is carried out during the positive half cycle of the input voltage. Moreover, the proposed rectifiers operation in Fig. 1 will be described assuming that the three inductors are operating in DCM. Operating the rectifier in DCM, have several advantages. The main advantages includes natural near-unity power factor, the switches are turn ON at zero current, and the output diodes (*Do*1 and *Do*2) are turned OFF at zero current. Thus, the turn-ON switching losses and the reverse recovery of the output diodes are considerably reduced. Conversely, DCM operation significantly increases the conduction losses due to the increased current stress through circuit components. As a result, this leads to one disadvantage of the DCM operation, which limits its use to low-power applications (<300 W). Similar to the conventional Cuk converter, the circuit operation in DCM can be divided into three distinct operating

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stages during one switching period *Ts*. The topological stages of cuk rectifier over a switching cycle can be briefly described as follows, *Stage 1[t_0, t_1], [Fig. 2(a)]:* This stage starts when the switch Q_1 is turned ON. Diode D_p is forward biased by the inductor current i_{L1}. As a result, the diode D_n is reverse biased by the input voltage. The output diode D_{o1} is reverse biased by the reverse voltage (v_{ac} + V_o), while D_{o2} is reverse biased by the output voltage V_o. In this stage, the currents through inductors L_1 and L_{o1} increase linearly with the input voltage, but the current flowing through inductor L_{o2} is zero due to the constant voltage across C_2 . The inductor currents of L_1 and L_{o1} during this stage are given by,

diLn/dt = vac/Ln……(1)

Accordingly, the peak current through the active switch Q_1 is given by,

IQ1,pk = (Vm/Le)D1TS……..(2)

Where V_m is the peak amplitude of the input voltage v_{ac} , D_1 is the switch duty cycle, and L_e is the parallel combination of inductors L_1 and L_{o1}. *Stage 2[t_1, t_2] [Fig. 2(b)]:* This stage starts when the switch Q_1 is turned OFF and the diode D_{o1} is turned ON simultaneously providing a path for the inductor currents i_{L1} and i_{Lo1} . The diode D_p remains conducting to provide a path for i_{L1} . Diode D_{o2} remains reverse biased during this interval. This interval ends when i_{Do1} reaches zero and D_{o1} becomes reverse biased. Note that the diode D_{o1} is switched OFF at zero current. The current through inductor L_1 and L_{o1} during this stage can be,
represented as follows:

(diLn/dt)= − Vo/Ln,……(3)

Stage 3[t2, t3] [Fig. 2(c)]: During this interval, only the diode *Dp* conducts to provide a path for *iL* 1 . Accordingly, the inductors in this interval behave as constant current sources. Hence, the voltage across the three inductors is zero. The capacitor *C*1 is being charged by the inductor current *iL* 1 This period ends when *Q*1 is turned ON. By applying inductor volt-second across *L*1 and *Lo* 1 , the normalized length of the second stage period can be expressed as follows:

D2 = (D1/M) sin ωt ……..(4)

where ω is the line voltage angular frequency, and *M* is defined at the voltage conversion ratio (*M* = *Vo* /*Vm*). Since the diode *Dp* conducts throughout the entire switching period, the average voltage across *C*2 is equal to the output voltage *Vo* . Due to this, a negligible ac current will flow through *C*2 and *Lo* 2 . The current flowing through *L*2 during the positive half cycle of the input voltage is equal to the negative current through the body diode of *Q*2 . It should be noted that the body diode of the inactive switch *Q*2 is always conducting current during the positive half cycle of the input voltage. The reason is due to the low impedance of the input inductors (*L*1 and *L*2) at the line frequency. Therefore, the input diode *Dp* and body diode of *Q*2 appear in parallel configuration to share the return current. A large portion of the return current will pass through the diode that has a lower voltage drop. The efficiency of the proposed converter can improved by using synchronous rectification to turn ON the switch *Q*2 during the positive half cycle of the input voltage, which eliminates its body-diode conduction.

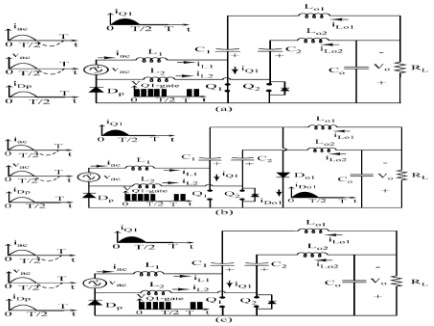

Fig. 2. Topological stages over one switching period Ts[1]

The Cuk converter offers several advantages in PFC applications, such as it is easy to implement in transformer isolation, protection against inrush current occurring at start-up or overload current, lower input current ripple, and less electromagnetic interference (EMI) associated with the discontinuous conduction mode (DCM) topology.

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III. CONVERTER DESIGN

Let,
Input voltage, Vac= 100Vrms,
Output V_0=48V,
Power, P=150W
P=V×I…….. (5)
150=48×I
Therefore, output current I=3.125A
V_0=I×R,……(6)
48=3.125×R,
R=15.34 Ω
Select Switching frequency, F=4 kHz
Output voltage ripple should be <1%
$\Delta i_{L1}<10\%I_{L1}$
$\Delta Vc_1<5\%Vc_1$

$$\Delta i_{L1}=\frac{D.Vin}{F.L1}$$ …… (7)

Δi_{L2}= (1-D) Vo/ (F.L_2)……..(8)
ΔVc_1 = (D.V_d i_d) / (Vo.C.F)……..(9)

From equation (7) ,(8) and (9) gives the values of inductance and capacitance,

L_1= L2=1mH
L_{01}=L_{02}=22µH

C_1=C_2=1µF

C_{out}=12000µF

Basic block diagram of cuk converter for power factor correction is shown in fig.3. The block diagram comprises, rectifier, cuk converter, inverter for converting dc into ac before fed into loads. A PFC controller is used to sense the

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load voltage and current variations and control the switching pulses to cuk accordingly.

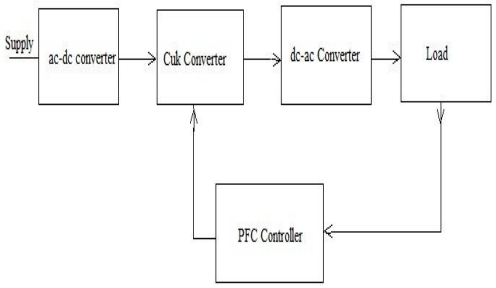

Fig.3. Block diagram for power factor correction

IV. SIMULATION MODEL AND RESULTS

The modeling of proposed Cuk converter for PFC correction is done using Matlab/Simulink. Simulation model for the proposed Cuk Converter is shown in Fig.4.

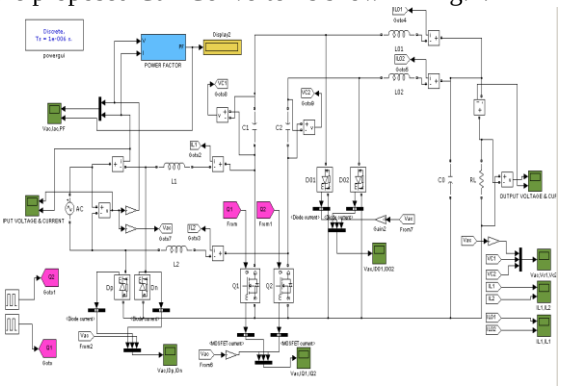

Fig.4.Simulation model

Simulated waveforms of proposed converter is shown in figures. Waveforms shown below are corresponds to the converter when operating in discontinuous mode of operation.

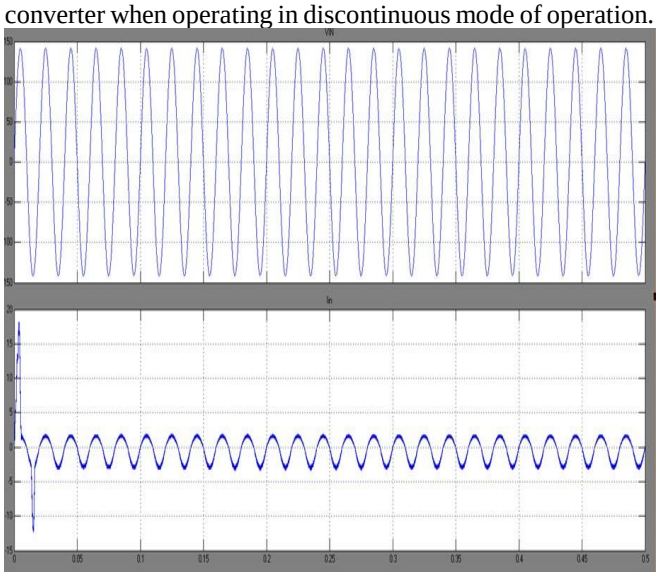

Fig.5.Input voltage and Current Waveforms

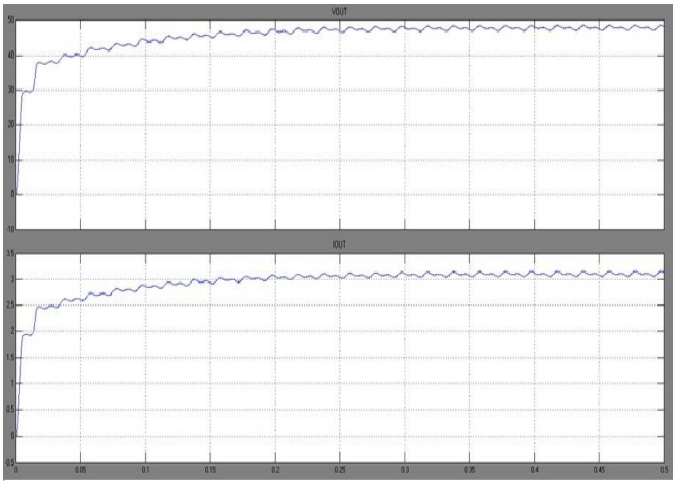

Fig 6.Output voltage and current waveform

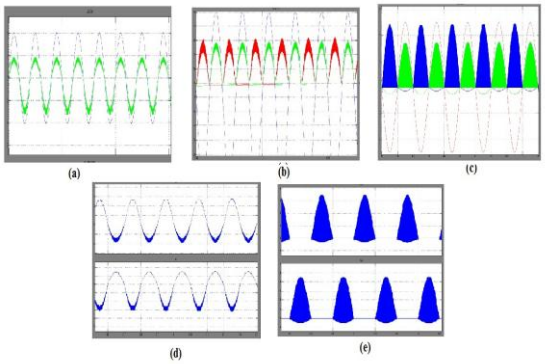

Fig.7. (a) source voltage and current, (b) V_{c1} & V_{C2}, (c) V_{Q1}& V_{Q2}, (d) I_{L1} & I_{L2}, (e) I_{L01} & I_{L02}

V. CONCLUSION

The single-phase ac–dc bridgeless rectifiers based on Cuk topology are presented and discussed. The validity and performance of the proposed topology was verified by Simulation. Since conduction and switching losses are less, the proposed topology can further improve the conversion efficiency when compared with the conventional Cuk PFC rectifier.

VI. ACKNOWLEDGMENT

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